Demonstration of a 0.48 THz Amplifier Module Using InP HEMT Transistors

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***Abstract*—In this letter, we present an amplifier module operating at a frequency of 0.48 THz. This represents almost a 50% increase in solid-state amplifier operating frequency compared to prior state of the art, and is the highest reported amplifier to date. The amplifier demonstrates a peak gain of 11.7 dB measured in a waveguide split-block housing. Sub 50-nm InP HEMT transistors with an estimated $f_{MAX} > 1$ THz are used to achieve this level of performance. The five stage amplifier is realized in coplanar waveguide, and uses monolithically integrated dipole probes to couple the chip from the WR 2.2 waveguide.**

***Index Terms*—Coplanar waveguide, HEMT, low noise amplifier, MM-wave, MMIC, sub-millimeter wave.**

I. Introduction

THE sub-millimeter wave regime begins at frequencies above 300 GHz where wavelengths are less than 1 mm. Traditionally, receiver applications at short mm-wave frequencies to sub-millimeter wave frequencies, such as atmospheric sensing and radio-astronomy, have relied on mixer front-ends [1] and sophisticated technologies have been developed to support this [2]. Only recently have active electronics using solid-state technologies been demonstrated operating at sub-millimeter wavelengths in InP HEMT [3], MHEMT [4], InP HBT oscillators [5] and amplifiers [6], [7] with operating frequencies to 340 GHz. In this letter, we present a packaged amplifier operating at 480 GHz, representing approximately a 50% increase in the operating frequency of solid-state transistor amplifiers. The work itself relies on a sub 50-nm InP HEMT transistor, which achieves an f_{MAX} value > 1 THz [8]. This is a similar transistor technology to the one used in [3], but we use a 14 μm (7 μm per gate finger) transistor for operation at higher frequencies.

A microphotograph of the five stage amplifier in a split-block waveguide housing is shown in Fig. 1. The total amplifier die size is 0.9×0.32 mm^2, and includes structures for electromagnetically coupling the signal from the waveguide to the amplifier die, thus avoiding wirebonding. We have previously used monolithically integrated E-Plane probes [9], but have more recently experimented with a monolithic dipole transition that performs well on high permittivity substrates. The signal is coupled from the WR 2.2 waveguide to the chip by the monolithically fabricated dipole in a matter similar to that shown in [10].

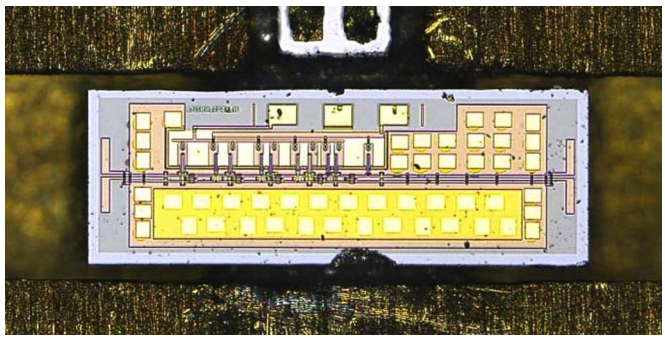

Fig. 1. Microphotograph of 480 GHz LNA in split block housing. The signal is electromagnetically coupled to the chip by monolithically integrated dipole probes.

II. THz InP HEMT Technology

Critical for realizing amplifiers at the target design frequency of 0.5 THz is a transistor with sufficiently high gain at the design frequency. To achieve the target operating frequency, we use an InP HEMT epitaxial profile with a composite InGaAs/InAs channel. This process has produced measured InP HEMTs with transconductance >2300 mS/mm, maximum channel current >900 mA/mm, MAG/MSG values as high as 14.5 dB at 110 GHz, f_{MAX} of 1.2 THz and f_T as high as 580 GHz at Vds = 1 V [8]. The devices have good pinchoff characteristics, good output conductance, and a breakdown voltage that allows for on-state device drain bias as high as 2 V and reverse bias 2-terminal breakdown voltage greater than 3 V. The MMIC process [8] employs two metal interconnection layers with a 2nd layer airbridge, precision thin film resistors and MIM capacitors. The 3" InP wafers are thinned to 25 μm thickness and grounding slot vias are reactive ion etched with a plated Ti/Au back metal.

A critical challenge as amplifier design frequencies increase is insuring that the transistor's model extrapolates well with frequency. With VNA frequency extenders and wafer probes commercially available to 325 GHz, it is in principle possible to obtain transistor S-Parameter measurements to these frequencies; we have found transistor measurements below 110 GHz to be most accurate and repeatable for transistor modeling. For design, transistor performance is then extrapolated to the design

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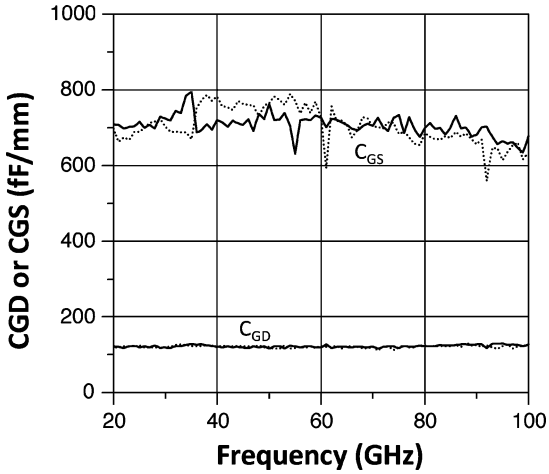

Fig. 2. Two extractions of CGS and CGD with successive calibration and measurements.

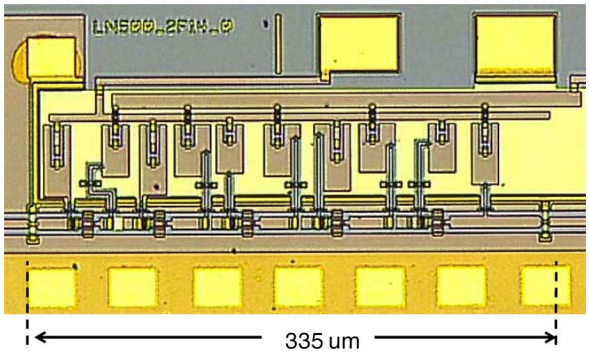

Fig. 3. Microphotograph of amplifier portion of chip.

frequency of 500 GHz. Shown in Fig. 2 are two repeated extractions of C_{GS} and C_{GD} from the measured transistor S-Parameters after converting to Y-Parameters and normalizing to 1 mm. For the small transistor size, the extractions are flat and repeatable to even 100 GHz.

III. Amplifier Design

The design goal of the amplifier is to obtain a high amount of broadband gain to an upper frequency of 500 GHz. We use a 14 μm transistor with two 7 μm fingers to avoid distributed effects, the smallest transistor size that we have used to date in our amplifiers. Simulations of the transistor model scaled to 14 μm show a MAG/MSG of 7–8 dB, where the range is provided based on measurements performed on different lots of our sub 50-nm HEMT process extracted over the last two years. Note that the model is extracted from S-Parameter measurements performed to 110 GHz on 30 μm transistors, and then extrapolated to 100 GHz after scaling the model to the 14 μm size used in the design.

A detailed microphotograph of the amplifier portion of the chip is shown in Fig. 3. Small shunt MIM capacitors are used for input and output matching. Due to the small capacitance and inductance of the 14 μm transistors, both the input and output load match are well behaved and lie close to the 50 Ω admittance circle with only a simple shunt connected CPW transmission

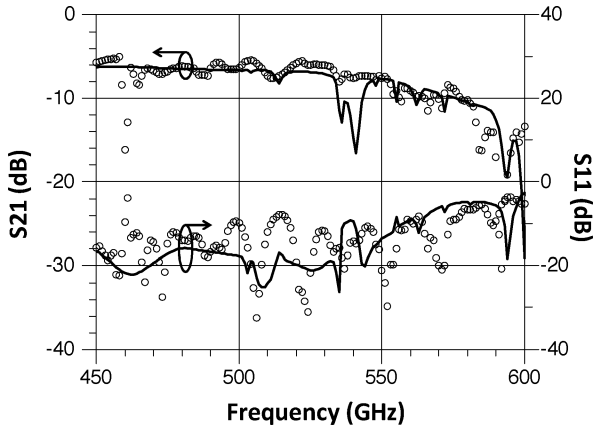

Fig. 4. Measured S-Parameters of "through" structure to validate WR 2.2 dipole transition. Note that solid lines indicate simulated performance and circles indicate measured performance.

line necessary for an optimal gain match. Transmission lines under a quarter wavelength at 500 GHz, with the longest CPW matching element were only 50 μm.

The amplifier portion of the chip detailed in Fig. 3 consumes 335 μm of the total 900 μm chip length, or slightly less than 70 μm per stage for the five stage amplifier. Referring again to Fig. 1, approximately 300 μm of 50 Ω CPW line is present between the amplifier portion of the chip and the output transmission line. The remaining 300 μm of the chip length is taken up by the input and output transitions to waveguide.

The transition itself is similar to the dipole transition demonstrated in [10]. The width of the waveguide channel flares out from 279 μm to accommodate the 320 μm wide chip. The chip is mounted on a pedestal which suspends the dipole portion of the chip in the air. The backside metal of the MMIC is patterned so that no metal is present behind the dipole. When the split block lid is placed on top of the chip, the remaining space above the chip is cutoff. The channel formed in the chip itself by the 25 μm thick InP substrate with grounding on the top and bottom must also be cutoff for the parallel plate waveguide mode. This is accomplished by using densely placed substrate vias, which are visible in the bottom portion of Fig. 1. At the input and output of the chip, a dense row of vias is used to reflect incident power back to the dipole.

IV. Measurements

Full 2-Port S-Parameter measurements performed on the package amplifier. This was done using a set of prototype WR 1.5 frequency extension modules developed by Virginia Diodes, Inc. Although the WR 1.5 waveguide band starts at 500 GHz, we are operating it to a start frequency of 460 GHz because we do not currently have a WR 2.2 testset available. The frequency extension modules were calibrated using a waveguide TRL calibration kit, also develop by Virginia Diodes.

Measurement validation of the WR 2.2 housing is shown in Fig. 4. The validation is performed by measuring the 2-Port S-Parameters of the housing with a CPW through line mounted rather than the amplifier chip. Measured and modeled performance is shown, where the modeled performance is obtained by HFSS. Estimated loss of the CPW through line is approximately 3 dB at 500 GHz for the 750 μm long section of CPW.

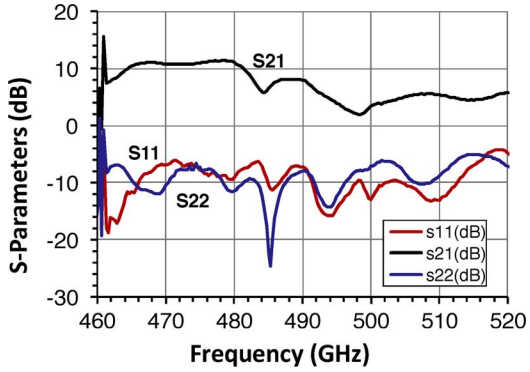

Fig. 5. Measured S-Parameters of amplifier module.

From Fig. 4, we estimate that the insertion loss from waveguide flange, to the inner edge of the dipole transition is $\sim$1.5 dB.

Measured performance of the fixtured amplifier is shown in Fig. 5. Measured gain greater than 10 dB is obtained from 465–482.5 GHz and peak gain of 11.7 dB is obtained. Referenced to the MMIC itself, $\sim$14.7 dB of gain is present if we subtract the estimated waveguide and transition losses, and $\sim$16.2 dB is present in the 335 μm amplifier portion if we subtract the excess 300 μm of CPW line loss at the output of the MMIC seen in Fig. 1. That yields $\sim$3.25 dB realized gain per transistor for the five stage design. Note that the peak in the gain at 462 GHz is due to the testset and was present before applying bias. The dip at 485 GHz is caused by a resonance in the housing due to the relatively fewer substrate mode suppression vias in the amplifier chip compared to the CPW through line chip. In the future we intend to improve the gain bandwidth and flatness by increasing the density of substrate mode suppression vias.

V. Conclusion

In this letter, an amplifier module operating at 0.48 THz has been presented. The amplifier uses InP HEMT transistors with an $f_{MAX} > 1$ THz [8] to reach this level of performance. The amplifier demonstrates that amplification from solid-state amplifiers is possible at significantly higher frequencies. We expect that as transistor performance continues to improve and as sub-millimeter wave amplifier design methodologies mature, solid-state amplification will continue to push towards Terahertz frequencies.

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