A High Power-Efficiency D-Band Frequency Tripler MMIC With Gain Up to 7 dB

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***Abstract*—A novel frequency tripler consisting of a harmonics generating stage and a converting stage is proposed. A common-emitter transistor in the first stage is used to produce mainly the first to third harmonics, while, a common-emitter transistor in the second stage converts simultaneously the first and the second harmonics into the third harmonic, and also amplifies the third harmonic at the input. The third harmonics obtained from different mechanisms add in favorably phase, and consequently improving the tripler's conversion gain. A proof-of-concept circuit is designed and manufactured in a 0.25 μm InP DHBT Technology. The tripler has a conversion gain between 0 dB to 7 dB in the output frequency range from 110 to 155 GHz. It demonstrates also up to 30 dBc rejection ratio of the undesired first, the second and the fourth harmonics. The tripler consumes a dc power of only 45 mW, and achieves a state-of-the-art peak power efficiency of 20.2%, which to the authors' knowledge, is the highest obtained among triplers with positive gain published so far.**

***Index Terms*—DHBT, frequency multiplier, InP.**

I. Introduction

FREQUENCY multipliers are often used in micro/millimeter-wave transceivers, to produce a high frequency LO signal for the mixer. A passive multiplier utilizing heterostructure barrier varactor (HBV) [1] or Schottky diode [9] generates high order harmonics, which does not dissipate dc power. However, it suffers from conversion loss and requires a high input power. For example, a W-band HBV tripler has a conversion loss of 6.4 dB, and needs an input power as high as 29 dBm [1]. Consequently, a power amplifier has to be used. The power efficiency of the whole LO chain will consequently be much worse than 23% obtained by HBV tripler itself [1]. Here the power efficiency is defined as $\eta = P_{\rm out}/(P_{\rm DC} + P_{\rm in})$; $P_{\rm out}$ and $P_{\rm in}$ denote the output and input power at frequency of $3f_0$ and f_0, respectively, $P_{\rm DC}$ denotes dc power consumption.

In contrast, an active multiplier, including a power amplifier sometime, can provide positive conversion gain with low input power. The desired harmonic generated by common emitter/source transistors is extracted by using either a filter [2]–[5], [10] or an injection-locked VCO [6]. Other kinds of active multipliers are based on a conventional mixer [7] or a $\times 2$ sub-harmonic mixer [8], to generate double or tripler frequency signal, respectively.

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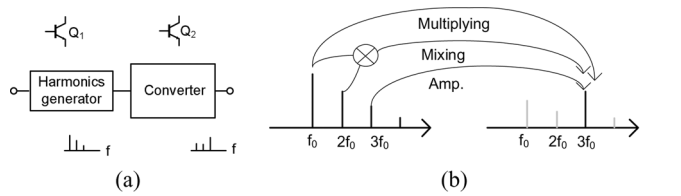


Fig. 1. (a) Proposed two stages tripler; (b) in the second stage, the third harmonic ($3f_0$) originates from different sources.

Unfortunately, most of the active multipliers have poor power efficiency. For example, the frequency doublers in [2]–[4] have power efficiency less than 7.4%, and triplers in [6] and [10] have power efficiency of 0.6%, and 1.4%, respectively. On the other hand, the conversion gain of the multipliers for output frequency above 90 GHz is also quite low, the best conversion gain obtained is about 3 dB among the multipliers in [2]–[7].

To improve the conversion gain and power efficiency, a novel two-stage tripler is proposed, as shown in Fig. 1(a). In the first stage, a common-emitter transistor is used to generate the different harmonics, dominated by the first to the third harmonics. In the second cascaded stage, a common-emitter transistor is employed, to convert the first and the second harmonics into the third harmonic and to amplifying also the third harmonic directly, as shown in Fig. 1(b). Adding up all those contributions, it is possible to improve the tripler's conversion gain.

Furthermore, the transistor at the first stage operates in class-B configuration in a harmonic-rich manner, while the transistor at the second stage operates in class-B/C configuration which demonstrates strong nonlinearity. In this case, the two transistors consume quite small dc current and therefore, good power efficiency is achieved.

II. Circuit Analysis and Design

A. Principle of Operation

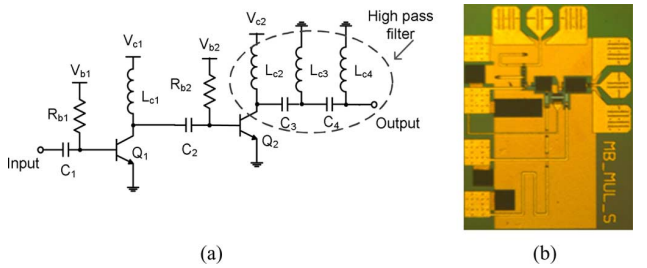
The principle of the harmonic generating stage is the same as that of a multiplier based on a common-emitter transistor [2]–[5], which will not be discussed here.

However, it is difficult to investigate the operation of the second stage by an analytic method. Instead, harmonic balance simulations will be carried out in order to understand the contributions of each mechanism to the tripler's output. Namely, the third harmonic obtained by means of multiplying, amplification, as well as mixing, will be calculated separately. In the simulation, the input signal has a power of -2 dBm at a frequency of 50 GHz.

In the simulations, the frequency components generated at the first stage are removed intentionally by using a series connected

TABLE I
SIMULATED OUTPUT POWER AT DIFFERENT CASES

Function of Q_2	f_0	$2f_0$	$3f_0$	P_{out} (dBm)
Multiplication (×3)	Y	×	×	0.5
Amplification	×	×	Y	-11.6
Multiplication+Mixing	Y	Y	×	1.0
Multiplication+Mixing+Amp.	Y	Y	Y	1.5



(a) (b)

Fig. 2. (a) Schematic of the tripler; (b) Chip photography (size: 0.56 mm × 0.64 mm).

LC resonator with a ground terminal. In ideal case, the magnitude of impedance of the LC resonator is 0 Ω at the resonate frequency, and larger than 600 Ω at other harmonic frequencies. The LC resonator does not affect the impedance between two stages except at resonate frequency, since its impedance is much larger than the parallel connected base impedance of the second transistor.

First, two LC resonators with resonate frequency of $2f_0$ and $3f_0$ are used, thus, the input of the second stage is dominated by the first harmonic. The simulated power at $3f_0$ is 0.5 dBm via frequency multiplication $(\times 3)$ as shown in the Table I. Secondly, filtering out the first and the second harmonics, the third harmonic $(3f_0)$ at the input is amplified, and getting a power of -11.6 dBm (0.1 mW). Thirdly, taking away the third harmonic, in this case, the second stage has dual-function: 1) multiplying $(\times 3)$ the first harmonic; 2) mixing the first and the second harmonics. The simulated power at $3f_0$ is 1.0 dBm (1.2 mW). This value is larger than the power obtained by amplification.

Even though the gain of amplification can be increased by dissipating more dc current, the nonlinear converting has better power efficiency than the amplification since the second transistor operates in class-B/C configuration.

If keeping all harmonics at the input of the second stage in the simulation, we get a power of 1.5 dBm (1.4 mW) at $3f_0$, which is roughly equal to the sum of those obtained by the nonlinear converting (1.2 mW) and by the amplifying (0.1 mW).

B. Circuit Design

A proof-of-concept tripler operating at D-band output frequency was designed in a 0.25 μm InP DHBT process. Under optimal bias condition, the transistors are able to achieve f_t and f_{max} around 350 and 600 GHz, respectively. The tripler's schematic is shown in Fig. 2(a). The first transistor has two emitter fingers with a length of 10 μm; the second transistor has one finger. The sizes of two transistors and their biases are selected through optimization with a goal of maximum conversion gain.

The undesired first and second harmonics are suppressed by a fifth order Chebyshev high-pass filter which is built by capacitors, as well as transmission lines as inductors. The capacitances of C_3 and C_4 in the filter are 17 and 21 fF, respectively.

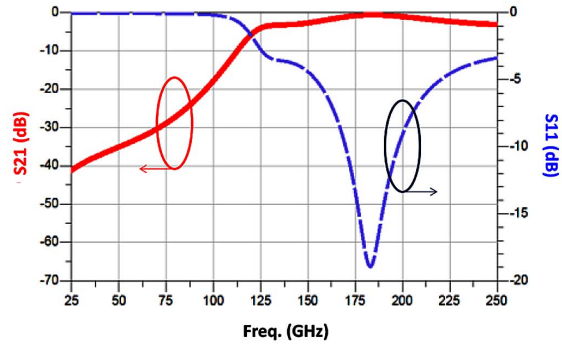


Fig. 3. Simulated S-parameter of the high-pass filter used in the tripler.

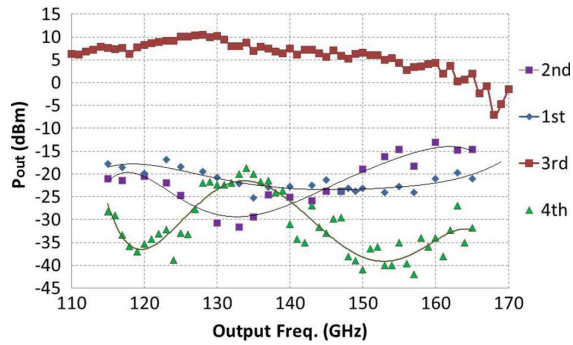


Fig. 4. Measured output power of the first, the second, the third, and the fourth harmonics, where thin solid lines represent polynomial data fitting curves for the first, the second, and the fourth harmonics.

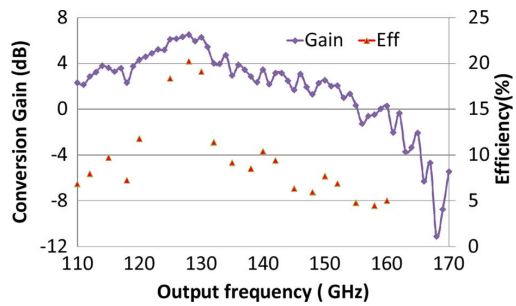


Fig. 5. Measured conversion gain and power efficiency.

The transmission lines, L_{c2}, L_{c3}, and L_{c4}, have the same width of 6 μm, and a length of 105 μm, 65 μm, and 185 μm, respectively. The size of the filter is 110×109 μm^2. The simulated S-parameter of the filter is shown in Fig. 3. The minimum loss in the pass-band is 0.6 dB.

III. TRIPLER MEASUREMENTS

The tripler's chip photo is shown in Fig. 2(b). The chip size is 0.36 mm^2, which is the smallest among the multipliers in [1]–[7], [10] partly due to the used multilayer technology.

On-chip measurements are carried out. The output powers at the first, the second, the third, as well as the fourth harmonics are measured. The input power is fixed at 3 dBm, and the frequency of the input signal is swept from 36.7 to 56.7 GHz, correspondingly to the output frequency at third harmonic from 110 to 170 GHz. The first and the second harmonic are measured using Agilent spectrum analyzer 8565EC and Preselected RF section HP 11974V. The third the fourth harmonics are measured using harmonic mixers SAM-170, SAM-220 and a signal source analyzer R&S FSUP, as well as an Erickson PM4 power meter.

TABLE II
SUMMARY OF MULTIPLIERS' PERFORMANCE (OUTPUT FREQUENCY >90 GHZ)

Ref.	Process	Outp. freq. Range (GHz)	Outp. Power (dBm)	Conv. Gain (dB)	Reject. (dBc)	Input power (dBm)	×N	P_{DC} (mW)	Eff. (%)	Chip Size (mm^2)
[2]	0.1μm InP HEMT	158 - 172	5	-2	--	7	×2	95.2	3.3	1.3
[3]	50 nm mHEMT	150 - 220	4.8	-7.2	--	12	×2	25	7.4	1.3
[4]	100nm mHEMT	110 - 130	5	3	--	2	×2	62.5	4.9	1.8
[5]	0.13μm SiGe HBT	215-240	-3	-3	--	0	×2	630	0.1	0.61
[6]	90nm CMOS	91~97	-12.5	-18.5	>17	-1	×3	5.5	0.6	0.49
[7]	2 μm InP DHBT	0~100	-11	1	>24	-9	×2	730	0.01	2.24
[10]	50nm mHEMT	140	-1.5	-11	--	9.5	×3	40	1.4	1.5
This work	**250nm InP DHBT**	**119-135**	**10**	**7**	**30**	**3**	**×3**	**45**	**12**	**0.36**

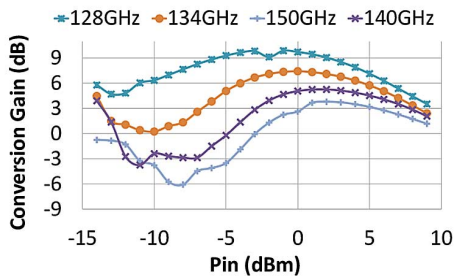


Fig. 6. Conversion gain versus input power at different frequencies.

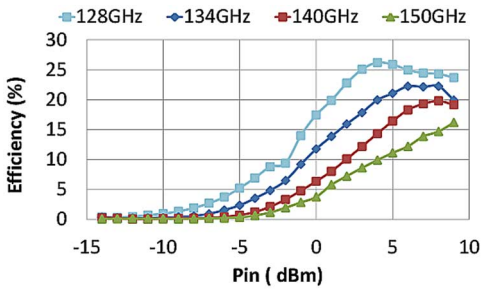


Fig. 7. Power efficiency versus input power at different frequencies.

As shown in Fig. 4, the tripler is able to deliver 10 dBm output power around 130 GHz. It demonstrates 30 dBc suppression of the first, the second, and the fourth harmonics. In the frequency range from 110 to 155 GHz, the tripler has an output power larger than 3 dBm, with minimum 20 dBc rejection ratio of the first, the second, and the fourth harmonic. The tripler's conversion gain is plotted in Fig. 5. Around 130 GHz, it achieves 7 dB conversion gain. This tripler has a 3 dB bandwidth from 119 to 135 GHz (12.6% relative bandwidth) and positive gain from 110 to 155 GHz.

The tripler consumes only 45 mW dc power at a collector voltage of 1.6 V. The base bias voltage for the first and the second transistor are 1.19 V and 0.9 V, respectively. The dc power dissipation of two transistors is comparable. The tripler's power efficiency is plotted in Fig. 5. It is larger than 12% in the 3 dB bandwidth from 119 to 135 GHz. The peak power efficiency is 20.2% at 130 GHz and input power 4 dBm.

The tripler's conversion gain depends on the input power, as shown in Fig. 6. The conversion gain peaks at a power of -2 dBm for 128 GHz signal and at 2 dBm for 150 GHz signal. This tripler is able to deliver maximum output power above 10 dBm ($\mathrm{P_{out}} = \mathrm{P_{in}} + \mathrm{Conv.\ Gain}$) with input power of 1 dBm at 128 GHz and 7 dBm at 150 GHz.

As shown in Fig. 7, the power efficiency is also a function of the input power. At a frequency of 128, 134, and 140 GHz, the power efficiencies are larger than 20%, at an input power larger than 1, 4, and 8 dBm, respectively.

Finally, the performance of the multipliers with output frequency higher than 90 GHz in the literature is listed in Table II. It can be seen that the proposed tripler achieves state-of-the-art power efficiency, conversion gain, and relatively high output power, as well as smallest chip size.

IV. CONCLUSION

A novel tripler consisting of two cascaded common-emitter transistors is demonstrated, featuring good conversion gain, relatively high output power, and very high power efficiency. it is able to deliver an output power larger than 10 dBm. Consequently, such a tripler is suitable to be used for the D-Band LO chain.

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