# A Phased Array RFIC With Built-In Self-Test Capabilities

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***Abstract*—An X-Band phased-array RF integrated circuit with built-in self-test (BIST) capabilities is presented. The BIST is accomplished using a miniature capacitive coupler at the input of each channel and an on-chip I/Q vector receiver. Systematic effects introduced with BIST system are covered in detail and are calibrated out of measurements. The BIST can be done at a rate of 1 MHz with 55 dB signal-to-noise-ratio and allows for the measurement of an on-chip array factor. Measurements done with BIST system agree well with S-parameter data over all test conditions. To our knowledge, this is the first implementation of an on-chip BIST with high accuracy.**

***Index Terms*—Built-in self-test (BIST), phase shifters, phased arrays.**

## I. Introduction

SILICON-BASED arrays have been demonstrated in transmit and receive modes for microwave and millimeter-wave applications. The All-RF architecture is predominant in phased-array designs due to its simplicity and its scalability to a large number of elements [1]–[12]. The silicon designs allow the integration of many channels on the same chip, together with the power combining network, and all the necessary digital control electronics. Recently, wafer-scale power combining arrays have been demonstrated at 90–100 GHz [13], and phased-arrays systems with a local oscillator, phase locked loop (PLL) and I/Q receiver (Rx) or up-converter (Tx) have been demonstrated up to 16 elements, and these form the basis of several Gbps communication systems [12], [14].

One of the key bottlenecks of RFIC-based phased arrays is the S-parameter testing of so many different channels on a single chip. This is typically done using expensive ground-signal-ground (GSG) probes and is time consuming. In fact, the cost of testing a phased array far exceeds the cost of the chip itself, especially at millimeter-wave frequencies [15]. The use of on-chip built-in self-test (BIST) capabilities would not only lower the testing cost, but will also allow the phased array to be tested in-situ and recalibrated versus temperature and aging. The BIST should be able to measure each channel individually and with high accuracy (better than the number of phase and amplitude bits required for proper operation) and should not reduce the RF performance of the chip (additional loss, NF, or coupling). Also it should be done in a short time (preferably $< 1\ \mu$s per measurement point) and should not occupy a large area on the RFIC. This paper presents the first on-chip BIST for an X-band phased array and with all the performance parameters listed above.

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## II. Built-In Self-Test System Design

### A. System-Level Description

The BIST can be designed in a variety of ways depending on the phased array chip functionality. Fig. 1(a) presents a phased array chip used in systems where the system-level transceiver is located at the sum port of the entire antenna (8–2000+ elements). In this case, a low power oscillator is integrated on-chip to provide the BIST test signal and is coupled to all the antenna ports using a $\sim$20 dB coupler. Each channel is then turned on individually and a compact I/Q receiver is integrated on-chip to measure the amplitude and phase of the injected signal, thus determining the channel vector response. Alternatively, the BIST signal can be provided from an external source and distributed to all the chips in the phased-array.

Fig. 1(b) presents a self-contained 8–16 elements phased-array communication (or radar) system with an integral oscillator and I/Q down-converter. In this case and during BIST operation, the local oscillator is routed to the antenna ports using switches, and the I/Q receiver is used to measure the channel response. The BIST systems in Fig. 1 are based on the homodyne approach, and therefore, the mixer I/Q outputs are mostly at DC. This is acceptable since the signal levels are high enough and the DC drifts can be normalized out of the measurements. For self-contained systems, the operational amplifier after the mixer can be part of the standard IF amplifier chain, or as a stand-alone unit that is engaged when the BIST mode is selected.

The BIST systems are shown in the receive mode, but similar BIST systems can be implemented for transmit or transmit/receive phased arrays or for systems using IF or LO beamforming [16]–[18]. It is also possible to build a heterodyne BIST system with a low intermediate frequency, but perhaps at the expense of higher power consumption.

The BIST should also be operational under two different conditions: 1) input ports left open-circuited and BIST is done on a low cost station with DC and low-frequency probes (testing a chip before use in an actual phased array) and 2) input ports connected to antennas and BIST is done "in the field". The difference between these conditions is the impedance seen at the

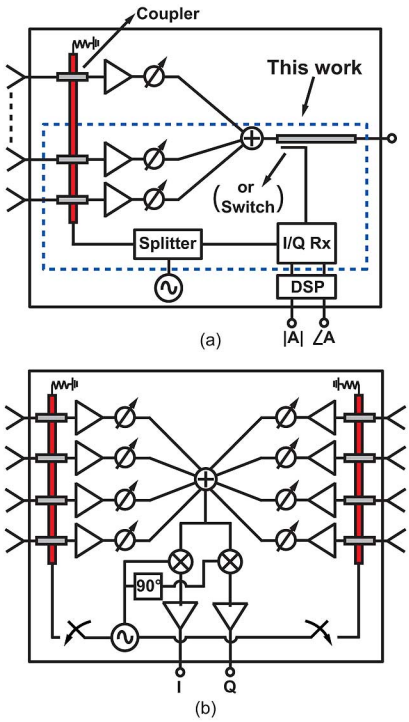



Fig. 1. BIST systems for (a) large phased arrays and (b) self-contained phased arrays.

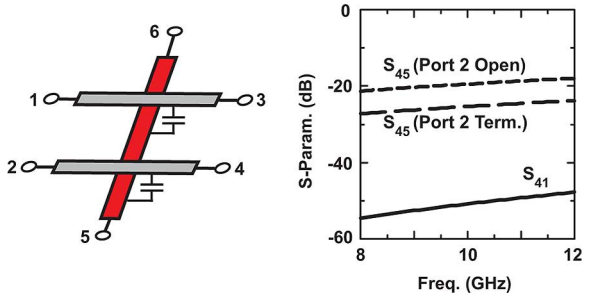



Fig. 2. Simulated S-parameters of a BIST-to-RF line capacitive coupler.

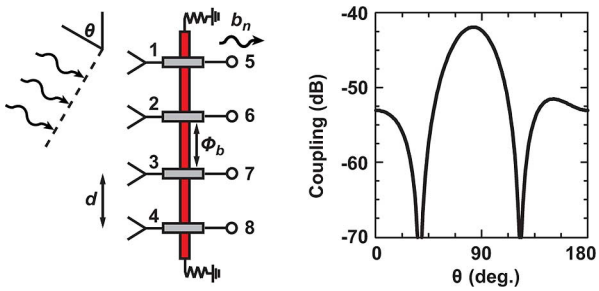



Fig. 3. Effect of BIST-to-RF couplers on phased-array channel-to-channel coupling ($\phi_b = 21°$, $d = 0.5\lambda_o$, $f = 10$ GHz).

RF input ports, which can affect the coupling value between the BIST line and the input ports. This will be discussed below.

### *B. BIST Couplers and Their Effect on Channel-to-Channel Coupling*

A key component in the BIST system is the compact coupler between the BIST transmission-line and the antenna port. The BIST line feeds all the antenna ports and is terminated with a matched resistor so as to eliminate any end reflections and result in an accurate coupling value. In fact, most of the power in the BIST line is coupled into this terminating resistor since the coupling value is low (-23 to -30 dB). There are two types of couplers that can be used: An electrically-small coupler that is capacitive or resistive in nature with no coupler directivity, or a transmission-line coupler with high directivity [19].

Fig. 2 presents a 2-channel system with a capacitive coupling mechanism (C = 34 fF). The same coupling value can be achieved if a $\sim 450\ \Omega$ resistor is used between the BIST and RF lines. In this case, the insertion loss is $< 0.1$ dB and the coupling value is $S_{45} = c = -26$ dB for a matched load at Port 2, but increases to $-20$ dB for an open-circuit load. A high-directivity coupler is not affected by the RF input port impedance and is a preferable choice, but it has 0.5–1 dB insertion loss, and requires a large area, which may not be compatible with a multi-element phased array.

The BIST-to-RF line coupling must be necessarily low since it also determines the coupling between the phased array channels on the same chip. For the case of standard operation (no BIST signal is engaged), the BIST couplers are still present and provide a leakage path between the phased array channels (Fig. 2). In this case, $S_{41} = S_{32} = -52$ dB for matched loads at all ports. While this may appear as sufficiently low coupling, care must be taken in phased-array operation. Consider a 4-channel array as in Fig. 3 with a BIST transmission-line delay $\phi_b$ between the ports and a coupling value of $c = -26$ dB (matched ports). For a plane-wave incidence angle of $\theta$ such that $\gamma = kd\cos\theta$, ($k = 2\pi/\lambda$, $d$ is the antenna-to-antenna spacing), the inputs at ports 1–4 are

$$a_1 = e^{-j0} \quad a_2 = e^{-j\gamma}$$
$$a_3 = e^{-j2\gamma} \quad a_4 = e^{-j3\gamma}.$$

Assuming $c \ll 1$ and after S-matrix manipulations

$$b_5 = 1 + c^2(e^{-j(\gamma+\phi_b)} + e^{-j(2\gamma+2\phi_b)} + e^{-j(3\gamma+3\phi_b)})$$
$$b_6 = e^{-j\gamma} + c^2(e^{-j(\phi_b)} + e^{-j(2\gamma+\phi_b)} + e^{-j(3\gamma+2\phi_b)})$$
$$b_7 = e^{-j2\gamma} + c^2(e^{-j(2\phi_b)} + e^{-j(\gamma+\phi_b)} + e^{-j(3\gamma+\phi_b)})$$
$$b_8 = e^{-j3\gamma} + c^2(e^{-j(3\phi_b)} + e^{-j(\gamma+2\phi_b)} + e^{-j(2\gamma+\phi_b)})$$

where the first term denotes the through signal coming from the antenna and the second term represents the power coupled to each channel through the BIST couplers. If $\gamma = \phi_b$ for a specific angle $\theta$, all coupling vectors are in phase for Port 8 and a maximum coupling of $|3c^2e^{-j3\gamma}|$ ($-42.5$ dB) is obtained for $c = 0.05(-26\text{ dB})$. In general, for an $N$-element phased array connected using a non-directional coupler line, the maximum voltage coupling is $(N-1)c^2$. Conversely, it is also possible to obtain a coupling value of $< -70$ dB, when all the coupling vectors cancel coherently for a specific angle (Fig. 3). It is therefore essential that the coupling, $c$, is low enough so that the total coupling is $< -35$ dB under all conditions and does not limit the phased-array performance.

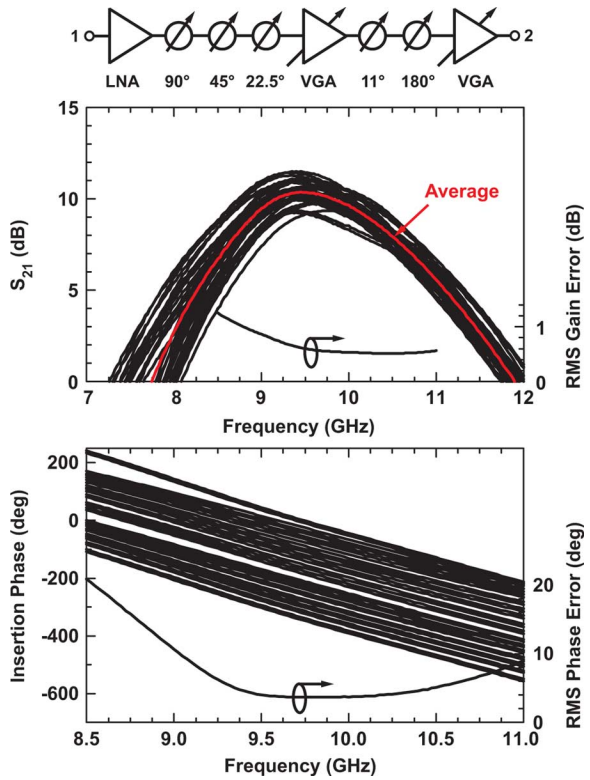



Fig. 4. Block diagram of the phased array channel and measured S-parameters.

### C. Other Applications of BIST

*On-Chip Phased Array Patterns:* The BIST transmission line feeds all channels at the same time, and therefore, an on-chip phased array pattern can be obtained if all the channels are turned on together and phase/amplitude controlled. This is also an ideal way to test the entire RFIC and find any asymmetry in the chip layout or power combiner.

*Frequency Response and Absolute Gain:* The BIST can also be used to determine the normalized frequency response, and the absolute gain can also be obtained with on-chip power detectors. However, as will be seen in Section V, the absolute gain is hard to measure accurately if a non-directional coupler is used and the RF ports are connected to antennas with a reflection coefficient of -10 dB.

## III. X-Band Phased Array With BIST: Building Blocks

### A. Phased Array Channel

The phased array channel design and Wilkinson power combiner were presented in detail in [20] and a short summary is included here. The chip is designed in the IBM8RF 0.13 $\mu$m CMOS process with $f_t = 100$ GHz and 8 metal layers. An amplifier/phase-shifter/amplifier approach is used with a center frequency of 9.5 GHz. The channel has a 5-bit phase shifter based on switched-LC unit cells, 3-bit gain control with a gain variation of 5–6 dB, an average gain of 10.3 dB, a NF of 3.5 dB and an input $P_{1dB}$ of $-13$ dBm, all at 9.5 GHz, and consumes 20 mA from a 1.8 V supply. The channel also provides input and output match of $< -10$ dB at 9–11 GHz. The measured on-chip S-parameters over the 32 phase states are shown in Fig. 4.

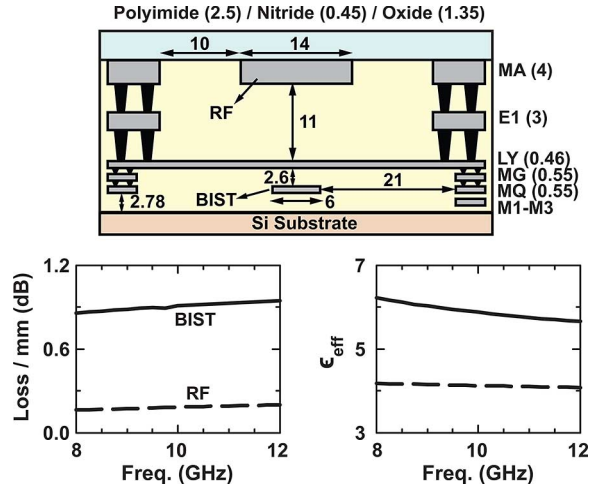



Fig. 5. The IBM8RF metal stack-up (all dimensions in $\mu$m) and simulated transmission-line characteristics of the embedded BIST and RF transmission lines.

### B. BIST Transmission-Line and Coupler

The RF transmission-line is built using a CPW configuration using the top metal layers (MA to LY) and the BIST transmission line is defined in the MQ layer below the RF line and ground plane (LY) (Fig. 5).

The BIST transmission line needs to feed multiple channels, and therefore it is important to simulate its insertion loss and propagation constant (Fig. 5). The BIST line has a simulated loss of 0.9 dB/mm at 10 GHz, and for a channel-to-channel spacing of 550 $\mu$m, the BIST signal at channel 1 is $-0.8$ dB and $-21^\circ$ as compared to channel 2. For 16-element chips arranged with 8-channels on each side, a difference of 3–4 dB exists between channel 1 and channel 8, and this can be calibrated out in the measurements.

The capacitive coupler is implemented by moving up the BIST transmission line to E1 layer and enlarging it underneath the RF line, and the overlap area determines the coupling value (Fig. 6). An overlap of $44 \times 76$ $\mu$m$^2$ results in a coupling value of $-26$ dB (all ports matched) and $-20$ dB (port 1 open circuited) at 9–10 GHz. The simulations are done using Sonnet, a full-wave electromagnetic simulator [21]. The BIST coupler has very little effect on the S-parameters of the RF CPW line, and the simulated $S_{31}$ is $< -0.1$ dB and is given by the CPW line loss (0.2 dB/mm at 9.5 GHz).

### C. BIST Circuits (I/Q Mixer, Op-Amp, Switch)

The BIST phased array chip block diagram is shown in Fig. 7 for a single channel test. Note that the Wilkinson power combiner has an additional 3 dB loss since the other channel is not active.

The BIST circuits need to occupy a small amount of area on the chip and therefore are implemented without any inductors (Fig. 8). For this demonstration, the BIST signal is generated off-chip and is fed using a GSG (CPW) probe. The signal is first divided between the BIST coupler line and the BIST LO line for the on-chip I/Q receiver using a wideband 3-port resistive

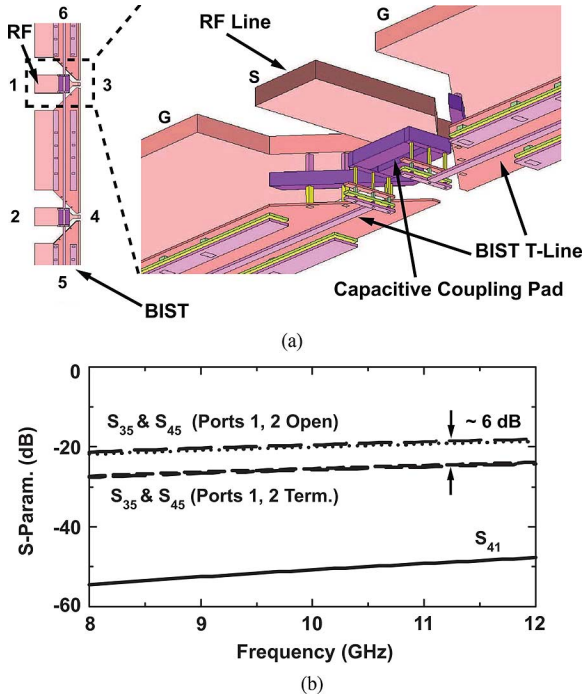



Fig. 6. Sonnet 3-D view and simulated S-parameters of the BIST coupler using back-end metal in IBM8RF process.

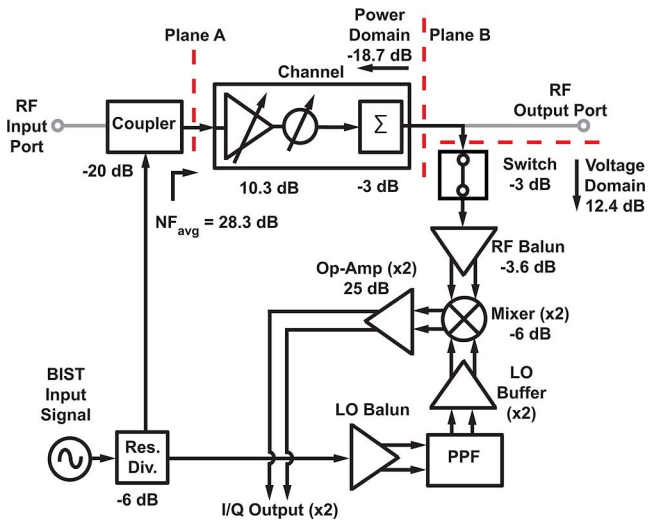



Fig. 7. The BIST phased array chip block diagram showing power or voltage gain of each block.

splitter with 6 dB loss. The I/Q receiver is based on differential passive mixers built using 0.13 $\mu$m CMOS with a simulated conversion loss of 6 dB. The BIST LO signal is amplified using an active balun, and a single-stage polyphase filter and limiting amplifiers are used to drive the I/Q mixers. The RF signal, coupled from the output of the chip, also passes by an RF active balun, and the signal is current divided into two paths (in phase) and fed to the I/Q mixers. Operational amplifiers, with a simulated closed-loop voltage gain of 25 dB and a 3 dB bandwidth of 3.15 MHz and built using wide CMOS transistors for low 1/f noise and are DC coupled to the mixer outputs. The Op-Amps have a closed-loop output impedance of 620 $\Omega$, and an output noise of 251 $\mu$V integrated over the entire 3 MHz bandwidth (needed for fast BIST operation). The noise is much lower if averaged over a narrower bandwidth using an off-chip DSP.

The I/Q down-converter consumes 30 mA from a 1.5 V supply with a simulated voltage gain of 15–12 dB at 8.5–10.5 GHz [Fig. 9(a)]. Due to the all-resistive design, the frequency response of the I/Q receiver is not constant vs. frequency, and it can be calibrated out of the measurements. The simulated BIST system results in $<0.6^\circ$ and $<0.3$ dB imbalance between the I and Q channel responses at 8–12 GHz, which is mostly due to device and layout mismatch. The input $\mathrm{P_{1dB}}$ at 9.5 GHz is $-9$ dBm at plane B (Fig. 7), which is more than enough for BIST operation. The BIST LO balun has a $\mathrm{P_{1dB}}$ of $-7$ dBm, and a power level of 0 dBm at the BIST input port is enough to drive the I/Q receiver.

The output BIST sampler (Fig. 8) can be designed using a 10 to 20 dB coupler or using a switched resistive load. A switch was chosen for improved signal to noise ratio (SNR) and to also provide a near 50 $\Omega$ impedance at the output port of the Wilkinson power combiner under standard operation and BIST conditions. This is achieved as follows: If the phased-array chip is tested without any termination on its output port (i.e., not connected to a phased array), then the CMOS switch is engaged and the switch on-resistance together with the 65 $\Omega$ and the input impedance of the RF balun provide a 50 $\Omega$ load to the Wilkinson power combiner and a coupling value of $-3$ dB. If a 50 $\Omega$ termination is present at the output port, then the CMOS switch is not engaged, and a $\mathrm{Z_{sh}}$ of 150-$j95$ $\Omega$ load at 10 GHz is connected in shunt across the RF line (Fig. 8). This results in an effective impedance of 40-$j5$ $\Omega$ at the Wilkinson output port (still matched to $< -17$ dB from 8 to 12 GHz), a coupling value of $-18$ dB and an RF insertion loss of 1.1 dB at 10 GHz. The added insertion loss may not be acceptable in certain systems, and a directional coupler could be a better choice at this location.

### D. BIST Signal-to-Noise Ratio

The signal power at plane A $(\mathrm{S_A})$ is $-26$ dBm for an input BIST signal of 0 dBm and an open circuit at the RF input port. The simulated single-sideband noise figure $(\mathrm{NF_{SSB}})$ at plane B is 38.5 dB [Fig. 9(b)] which translates to an $NF_{\mathrm{SSB}}$ of 28.3 dB at plane A due to the channel gain. This results in an equivalent noise power at plane A $(N_A)$ in a 3 MHz IF bandwidth of

$$\begin{aligned} N_A &= kT\left(\frac{\mathrm{dBm}}{\mathrm{Hz}}\right) + NF_{\mathrm{SSB}}\,(\mathrm{dB}) + BW(\mathrm{Hz}) \\ &= -174 + 28.3 + 64.8 \\ &= -80.9\ \mathrm{dBm} \end{aligned}$$

and the resulting SNR at plane A is

$$\mathrm{SNR}_A = \frac{S_A}{N_A} = 54.9\ \mathrm{dB}.$$

The output signal and noise voltages can also be calculated using a similar approach. For an input at plane A of $-26$ dBm at 9.5 GHz, the signal level at plane B is $-18.7$ dBm $(25.9\ \mathrm{mV_{rms}})$ and the output voltage (calculated as $\sqrt{(\mathrm{I}^2+\mathrm{Q}^2)}$) is 153.1 mV. The simulated output rms noise in a 3 MHz bandwidth is 194.7 $\mu$V, which results in an SNR of 54.9 dB.

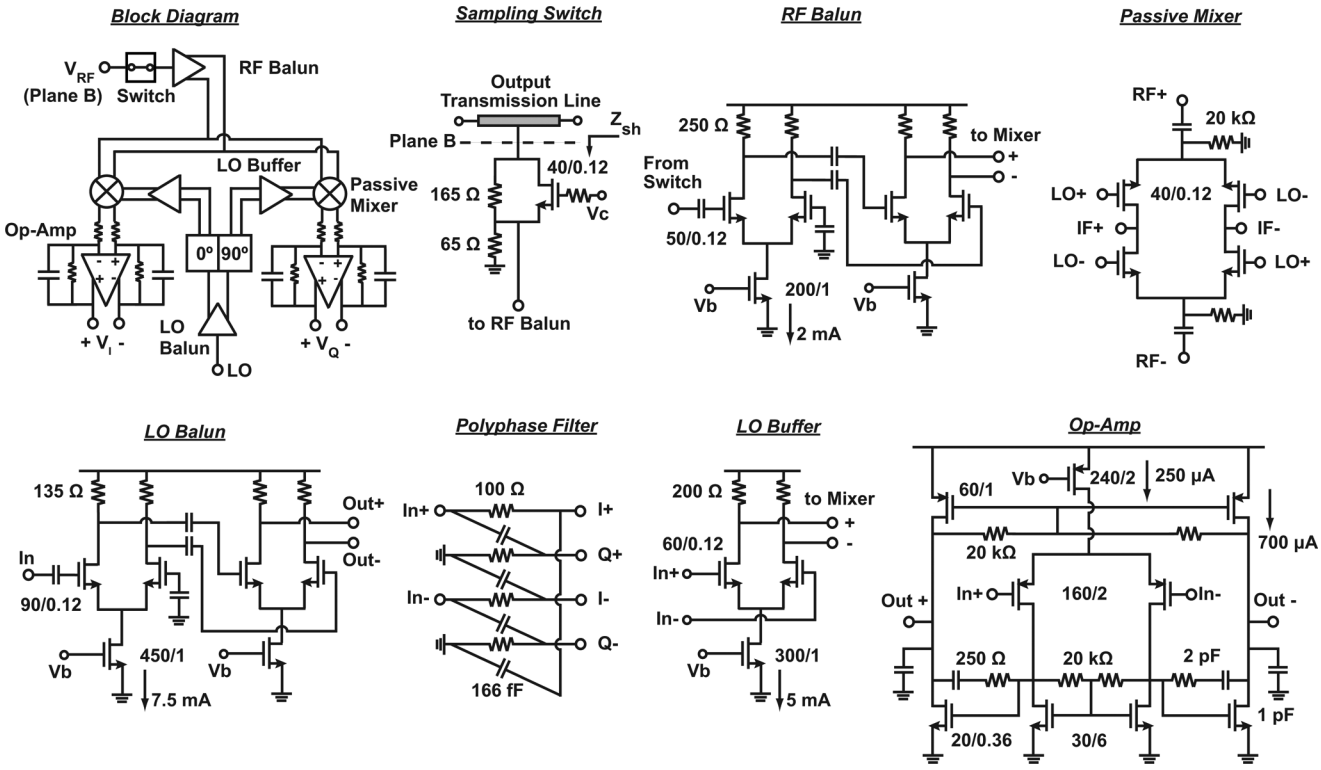



Fig. 8. Block diagram of I/Q receiver and schematics of blocks. All active transistors are biased through current mirrors and not shown here. All unlabeled capacitors are 1 pF.

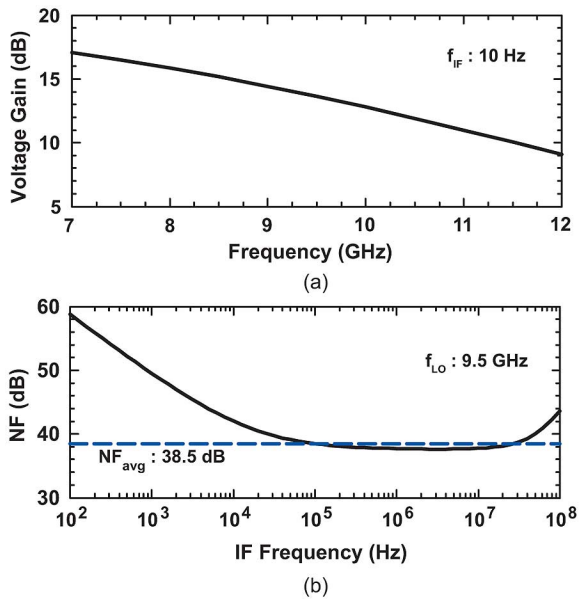



Fig. 9. (a) Simulated voltage conversion gain of receiver $(\mathrm{V_I}/\mathrm{V_{RF}})$. (b) Simulated noise figure of the BIST receiver at plane B.

The SNR is large enough to allow for a lower BIST input power ($-10$ dBm instead of 0 dBm) and very fast BIST operation in $< 1\ \mu$s testing speeds. The measured rms gain and phase errors using BIST with an LO power of $-10$ to $+10$ dBm are shown in Section IV.

## IV. Measurements

The 2-element phased-array chip with BIST is shown in Fig. 10. Note the BIST coupler, resistive splitter and BIST I/Q receiver.

### A. Individual Channels

The phased array response was measured using the BIST technique at 8.5–11.5 GHz with 250 MHz steps, but only few frequencies are shown for brevity. Fig. 11 presents the measured I/Q outputs at 9.5 GHz for all 32 phase states and a BIST input signal level of 0 dBm (channel 1 active and channel 2 turned off). The small steps in the I and Q voltages are not noise but actual change in the channel amplitude response at different phase states (the phase shifter has PM-AM conversion). The I and Q data are then processed externally to obtain the normalized amplitude and phase response using the standard formulas

$$A = \sqrt{I^2 + Q^2}$$
$$\text{Phase} = tan^{-1}\left(\frac{Q}{I}\right).$$

Fig. 12 presents a comparison of the measured BIST and S-parameter channel response versus phase states at 8.75, 9.5, and 10.25 GHz. The measurements are normalized to the $-90^\circ$ state (i.e., phase set to $-90^\circ$, average amplitude set to 0 dB) and the BIST measurements clearly predict the phase response and amplitude modulation due to the switched-LC phase shifters. Also, one can accurately measure the large jump in phase at 8.75 GHz due to the use of a high-pass/low-pass network for

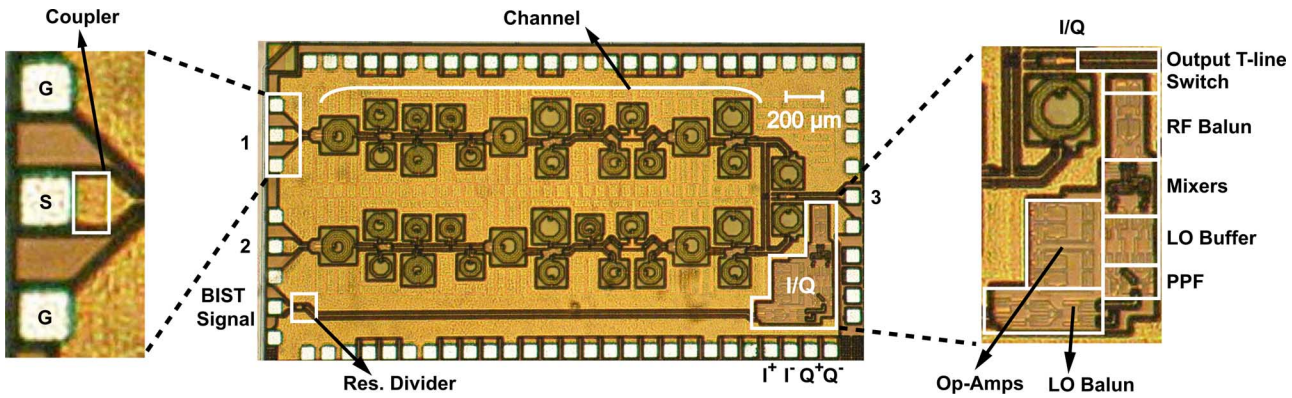



Fig. 10. Chip microphotograph of fabricated 2-channel phased array with BIST. Chip size is $2.95 \times 1.52$ mm$^2$.

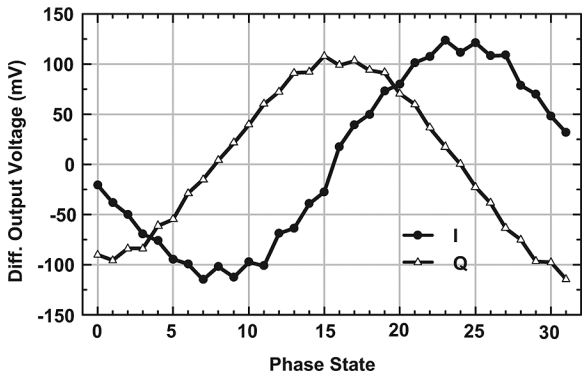
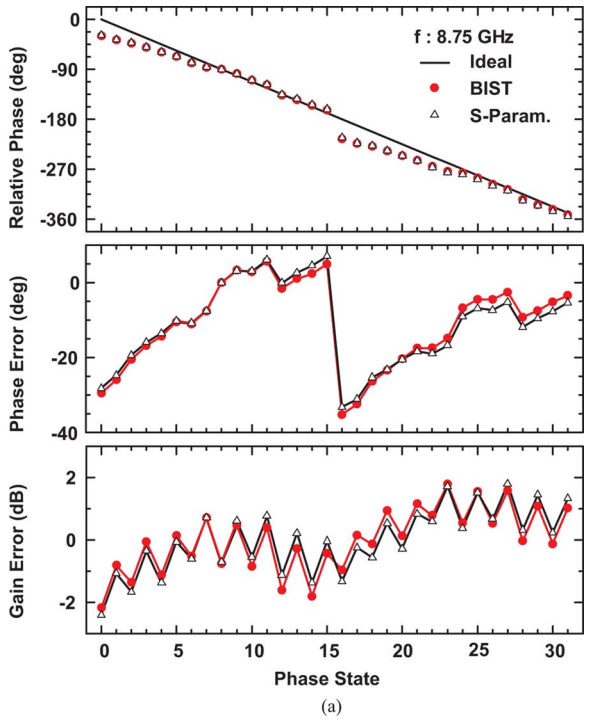



Fig. 11. Measured I and Q voltages at 9.5 GHz versus 32 phase states.




(a)

Fig. 12(a). Measured channel 5-bit response using BIST and S-parameters at (a) 8.75 GHz.

the 180° phase shifter cell and the use of a low-pass only network for the 11°, 22°, 45°, and 90° cells (more detail in [20]). The difference between the BIST and S-parameter phase measurements at 10.25 GHz is mainly due to the I/Q mismatch in the BIST receiver, since the center frequency of the I/Q polyphase network is designed to be at 9.5 GHz. The rms amplitude and phase errors can be calculated from the BIST measured data and agree well with S-parameter measurements (Fig. 13).

The frequency response can also be measured and is shown in Fig. 14 for two representative states (00111 and 10101). The response is normalized at 9.5 GHz due to the absence of on-chip power meters. Note that the BIST signal is higher at 8.5 GHz and lower at 10.5 GHz due to the frequency response of the BIST I/Q receiver with a maximum error of 1.9 dB. The gain control and any associated AM-PM conversion can also be measured using BIST and good agreement is obtained with S-parameter measurements (Fig. 15).

Channel 1 response was also tested versus the BIST signal level and no change in the channel response was observed other than an absolute level change in the output I and Q voltages. Fig. 16 presents the measured BIST rms gain and phase error versus BIST power level. The rms gain error reduces versus LO power due to compression in RF and LO BIST paths. Still the change is <0.1 dB and the BIST can be operated over a 20 dB power range.

The time domain response of the BIST system is shown in Fig. 17. In this case, the phase shifter is changed between two phase states with a 180° difference and the Op-Amp output was captured on an oscilloscope with 14 pF input capacitance. The measured 10%–90% fall time is 165 ns which results in an Op-Amp bandwidth of 2.1 MHz. The 90% system settling time is 235 ns, but this is not accurate enough for 5-bit phase shifter measurements since an 11° phase shift has $< 2\%$ amplitude modulation in the I and Q vectors. Therefore, it is important to quote the 98% settling time of 340 ns, and the BIST can be operated at 1 MHz rate with no problems. This means that an 8-element array can be tested in $<$ 1 ms over a wide range of amplitude and phase settings.

Measurements on channel 2 were identical to channel 1 and are not repeated. However, as expected, channel 2 shows 0.8 dB higher gain and a $+21°$ phase shift as compared to channel 1 (Fig. 18(a)—only I channel shown). This is due to the loss and the propagation constant of the BIST line, and agrees well with Sonnet simulations as shown in Fig. 18(b). In Fig. 18(b), the

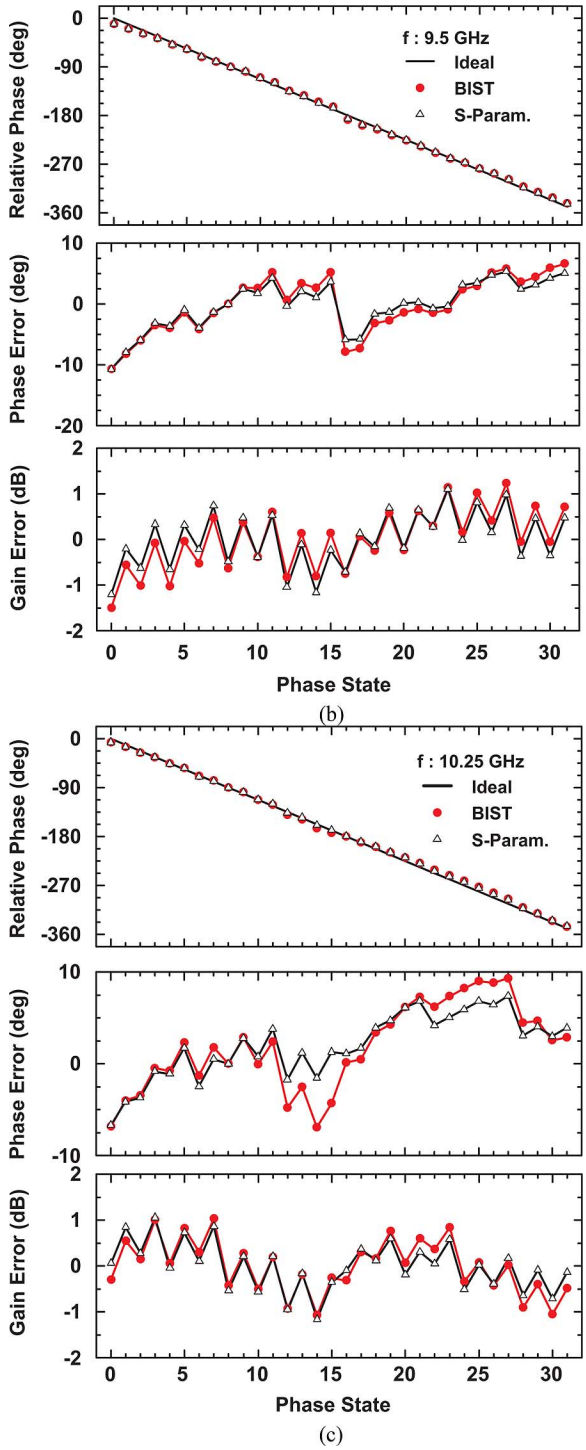



Fig. 12. *(Continued.)* Measured channel 5-bit response using BIST and S-parameters at (b) 9.5 GHz and (c) 10.25 GHz.

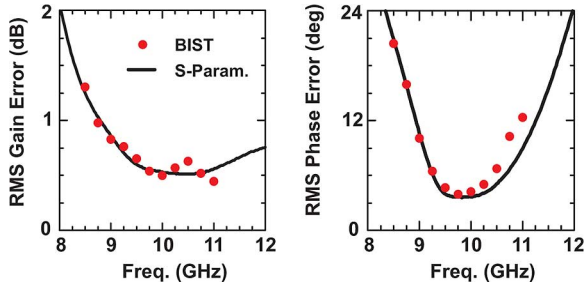



Fig. 13. Measured rms gain and phase error using BIST and S-parameters.

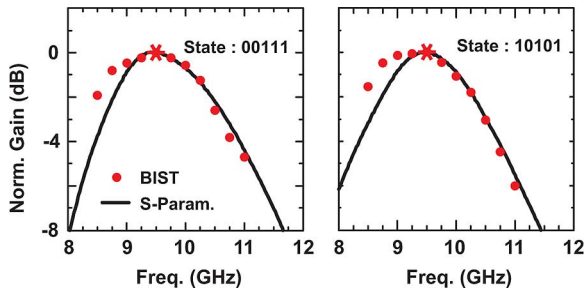



Fig. 14. Measured normalized frequency response using BIST and S-parameters for state 00111 and state 10101.

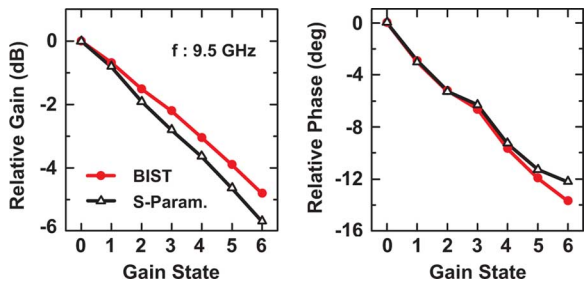



Fig. 15. Measured gain control using BIST and S-parameters: amplitude and phase.

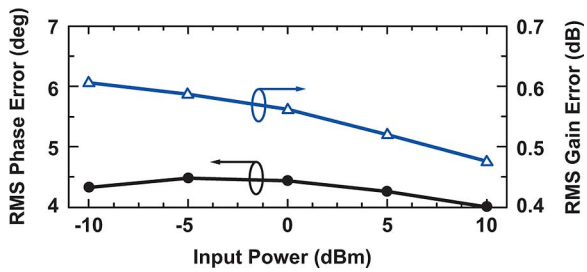



Fig. 16. Measured rms phase and gain error at 9.5 GHz versus BIST power level.

measured amplitude and phase difference is determined by comparing the amplitude and phase for the 0° phase states of the two channels. The 0.5 dB error at 8.5 GHz is due to an impedance mismatch at the phased array input port $(S_{11} = -7\ \text{dB})$ which changes the coupling between the BIST line and RF ports.

### *B. On-Chip Array Factor*

As mentioned above, one of the most useful features of BIST is the possibility to synthesize an on-chip array factor. In this case, both channels 1 and 2 are turned on and summed using the Wilkinson power combiner. The RF signal is then sampled using the BIST resistive coupler. Fig. 19(a) presents the measured I and Q voltages and Fig. 19(b) shows the corresponding amplitude response $(\sqrt{(I^2 + Q^2)})$ when the phase of channel 2 is set at 0° (state 00000) and 180° (state 10000) and the phase of channel 1 is changed from 0° to 360°. One can clearly see the 2-element array factor. Note the peak voltage is 235 mV which is twice that of a single channel as expected from a 6 dB power increase. This is due to the signals in the two channels adding

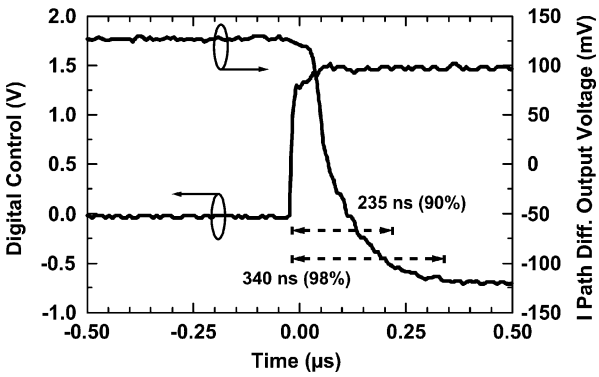



Fig. 17. Measured time domain response of BIST measurement.

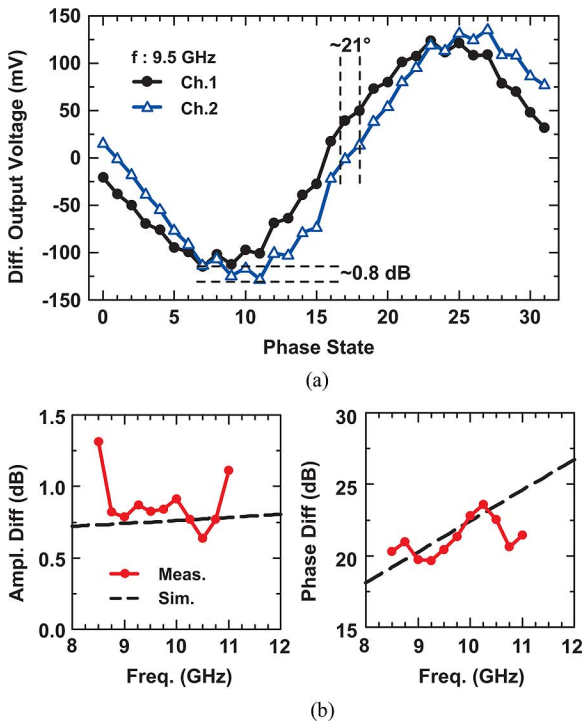



Fig. 18. (a) Measured channel 1 and channel 2 I-vector responses versus phase states at 9.5 GHz using BIST, and (b) measured amplitude and phase difference between channel 1 and channel 2 due to the BIST line.

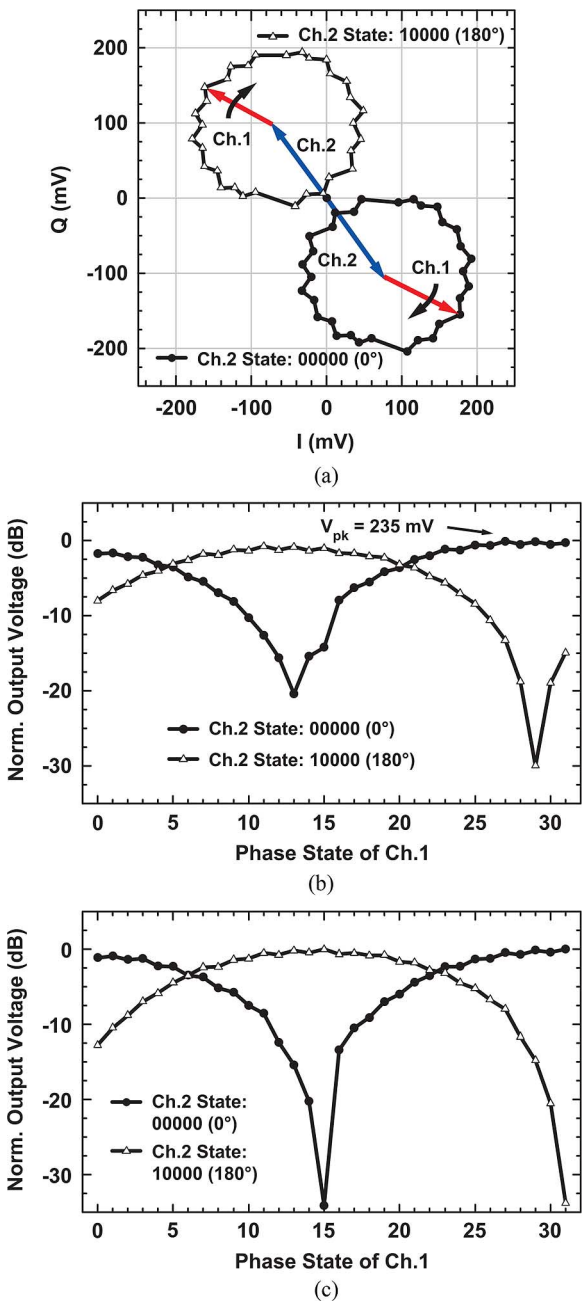



Fig. 19. (a) Measured I and Q voltages during array-factor measurements with BIST. (b) Measured 2-channel array factor using BIST at 9.5 GHz. (c) Synthesized 2-channel array factor at 9.5 GHz with the BIST line amplitude and phase difference calibrated out of measurement (see text).

coherently $(+3\ \mathrm{dB})$ and to the fact that the Wilkinson power combiner has an additional 3 dB of loss when a single channel is tested. The BIST phase difference between the channels, which is due to the finite length of the BIST line (21°) can be obtained from this measurement assuming that the channels' electrical lengths are identical. In the 0° case, perfect cancellation occurs when channel 1 is at 180°, but due to the 21° delay between the channels, cancellation occurs at state 13 (180°–22°). The BIST gain difference due to BIST line between the channels $(-0.8\ \mathrm{dB})$ can also be obtained by setting the channel phases 180° apart and adjusting the channel gains to obtain a deep null. However, the phase shifter PM-AM conversion must be first calibrated out from each channel since it is of the same order.

Fig. 19(c) presents the synthesized 2-channel array factor where the BIST transmission-line phase and amplitude difference is calibrated out of the measurements. In this case, perfect cancelation occurs at state 15 (180°) for 0° setting of channel 2. Also, the nulls in the calibrated on-chip array factor are much deeper than the un-calibrated case due to the correction of the 0.8 dB amplitude difference in the BIST line.

## V. Discussion

The BIST system can be used with calibrated power detectors to result in absolute gain and input $\mathrm{P_{1dB}}$ measurements which is very useful. This can be done using a calibrated power detector at the output port and is straightforward when the phased array chip is not connected to the antennas (stand-alone test mode). In this case, the coupling value can be simulated using Sonnet, is constant versus frequency and is not dependent on

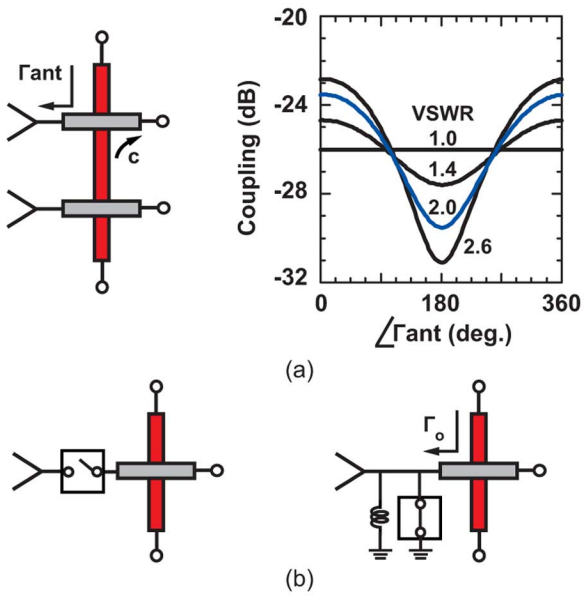



Fig. 20. (a) Effect of antenna port impedance on coupler performance and (b) proposed switch network for accurate gain measurements.

the RF port impedance (it is an open-circuit). However, when the chip is being used in a phased array system, the RF port impedance (or antenna impedance) depends on frequency and on the scan angle, and the coupling value is dependent on the RF port impedance since the lumped-element coupler does not have any directivity. Fig. 20(a) presents the simulated coupling value for a capacitive cross-over with $\mathrm{C} = 34$ fF($c = -26$ dB at 10 GHz when all ports are matched) and for an RF port VSWR of 1.0, 1.4, 2.0, and 2.6. The large variation in the coupling value, even at VSWR of 2.0, indicates that the simple capacitive (or resistive) coupler cannot be used to determine an accurate gain or a frequency response unless the RF port is well matched (-16 dB reflection coefficient).

The effect of the antenna impedance can be reduced with the use of CMOS switches. A series switch at the RF port isolates the lumped-element coupler when the BIST is engaged at the expense of additional loss [see Fig. 20(b)]. A shunt switch can also be used at the RF port, and can be resonated out using a shunt inductor when the BIST is not engaged which results in very low loss $(< 0.2$ dB$)$. However, when the BIST is engaged and the shunt switch is ON with a low impedance to ground $(10\ \Omega)$, the coupling value becomes $|c(1 + \Gamma_\circ)|^2 = -35.5$ dB (for $c = -26$ dB and $\Gamma_\circ = -0.66$) which may affect the system dynamic range. Of course, directional couplers at the RF port solve this problem and should be employed if space allows.

The proposed BIST technique can be extended to large arrays, but care must be taken to calibrate out the amplitude and phase difference between the channels. In this case and for an 8-element array, the amplitude and phase difference between channel-1 and channel-8 would be 5.6 dB and 147°, respectively. This difference can be predicted accurately using EM simulations and can be calibrated out of measurements. Another challenge in large arrays is the additional loss due to power combining network (for passive power combiners). Since only one channel is turned on during BIST operation, each Wilkinson power combiner presents an additional 3 dB loss, and this results in a 9 dB more loss for an 8-element array. Still, as long as the output SNR is sufficient for accurate measurements, the additional loss will not be a limitation.

## VI. Conclusion

This paper presented the first on-chip BIST for phased-array RFICs. The effect of BIST coupler on the phased-array performance is presented in detail and it is shown that, for non-directional couplers, it is important to have a low coupling value at the input of the chip. The BIST measurements agree very well with S-parameter measurements. It is expected that the BIST technique will be used in millimeter-wave phased arrays and will greatly reduce the RFIC testing costs.

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