Distributed MEMS True-Time Delay Phase Shifters and Wide-Band Switches

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***Abstract*— Wide-band switches and true-time delay (TTD) phase shifters have been developed using distributed microelectromechanical system (MEMS) transmission lines for applications in phased-array and communication systems. The design consists of a coplanar waveguide (CPW) transmission line ($W = G =$ 100 μm) fabricated on a 500-μm quartz substrate with fixed–fixed beam MEMS bridge capacitors placed periodically over the transmission line, thus creating a slow-wave structure. A single analog control voltage applied to the center conductor of the CPW line can vary the phase velocity of the loaded line by pulling down on the MEMS bridges to increase the distributed capacitive loading. The resulting change in the phase velocity yields a TTD phase shift. Alternatively, the control voltage can be increased beyond the pull-down voltage of the MEMS bridges such that the capacitive loading greatly increases and shorts the line to ground. The measured results demonstrate 0–60-GHz TTD phase shifters with 2-dB loss/118° phase shift at 60-GHz (~4.5-ps TTD) and 1.8-dB loss/84° phase shift at 40 GHz. Also, switches have been demonstrated with an isolation of better than 40 dB from 21 to 40 and 40 to 60 GHz. In addition, a transmission-line model has been developed, which results in very close agreement with the measured data for both the phase shifters and switches. The pull-down voltage is 10–23 V, depending on the residual stress in the MEMS bridge. To our knowledge, this paper presents the first wide-band TTD MEMS phase shifters and wide-band switches to date.**

***Index Terms*—MEMS, phase shifters, switches.**

I. Introduction

MICROELECTROMECHANICAL system (MEMS) switches have recently been developed for low-loss microwave and millimeter-wave control circuits such as single-pole single-throw (SPST) switches and switched-line phase shifters [1]–[3]. The advantage of using MEMS over FET's or p-i-n diodes is their low-loss performance and lack of measurable intermodulation distortion [4]. Current microwave MEMS switches have been fabricated in both series and shunt configurations. In the series configuration with the MEMS switch actuated (i.e., the top electrode pulled down), the signal path is completed, whereas in the shunt configuration, the signal path is shorted to ground with the switch actuated. In Goldsmith *et al.* [4], there is a thin dielectric layer on the bottom electrode to prevent a dc contact when the switch is actuated. This results in a capacitive switch suitable for 10–40-GHz applications. Yao *et al.* presented a metal-to-metal MEMS switch for use in systems up to 6 GHz [3]. MEMS switches have been fabricated in the fixed–fixed beam, cantilever, and diaphragm configurations, and the height is typically 3–4 μm above the transmission line, resulting in an actuation voltage of 25–100 V. Pacheco *et al.* have shown that low voltage actuation (14–16 V) can be achieved with a gap height of 3 μm by using serpentine and cantilever springs at the ends of the beam [5]. The 3–4-μm gap height is necessary in order to reduce the parasitic capacitance of the bridge in the OFF-state (bridge up), and results in a capacitance ratio ($C_{\text{down}}/C_{\text{up}}$) of 50–100 for capacitive switches. In the shunt configuration, the presence of the parasitic capacitance limits the high-frequency response of the switch in the OFF-state by producing unwanted reflections. In the series configuration, the parasitic capacitance limits the isolation of the switch by allowing coupling at high frequencies. MEMS switches have been demonstrated reliably up to 40 GHz with low insertion loss (0.2–0.5 dB) and high linearity [1], [4]. The achievable isolation with these switches is typically 20–40 dB, depending on the size of the MEMS bridge, with an associated reflection coefficient from -15 to -20 dB.

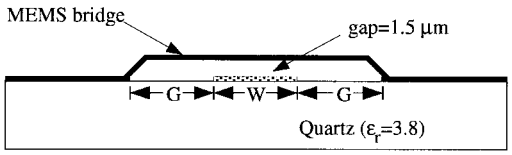

Fig. 1. Fixed–fixed beam MEMS bridge in shunt configuration over a CPW transmission line.

MEMS switch designs have been very similar to standard p-i-n diode or FET switch networks, with the active device replaced by the MEMS switch. This paper presents a departure from the traditional approach by incorporating the MEMS switches in distributed transmission-line designs. In this approach, a coplanar waveguide (CPW) transmission line is loaded periodically with the MEMS bridges, which act as shunt capacitors/varactors, as shown in Fig. 1. The impedance and propagation velocity of the slow-wave transmission line are determined by the size of the MEMS bridges and their periodic spacing. The shunt capacitance associated with the MEMS bridges is in parallel with the distributed capacitance of the transmission line [see Fig. 2(b)] and is included as a design parameter of the loaded line. Thus, the height of the MEMS bridges can be lowered from 3–4 to 1–1.5 μm. An immediate advantage of the lowered height is that the pull-down voltage of the MEMS bridges is reduced to 10–20 V. By using a single analog control voltage to vary the height of the MEMS

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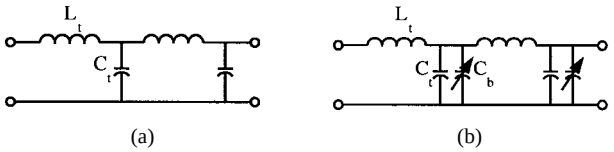


Fig. 2. Ideal (a) unloaded CPW line and (b) loaded DMTL's.

bridges, the distributed capacitive loading on the transmission line and, therefore, its propagation characteristics, can be varied. This results in analog control of the transmission-line phase velocity and, therefore, in a true-time delay (TTD) phase shifter (see Section III). Furthermore, if the MEMS bridges are pulled down (to form a very large capacitor), the distributed transmission line results in a wide-band switch (see Section IV).

It is important to note the work of Rodwell *et al.* on nonlinear distributed transmission lines (NLTL's). In this case, a CPW transmission line is loaded with millimeter-wave Schottky diodes and is used in voltage-level pulse shaping, picosecond-level sampling, and harmonic multipliers [6]. However, diode-based NLTL's are quite lossy, due to the series resistance of the Schottky diodes, and cannot be used in low-loss phase shifters and wide-band switches. For these applications, MEMS bridges offer excellent performance with very low additional transmission-line losses.

II. Distributed MEMS Transmission Lines

A. Design

The goal of this paper is the design and fabrication of distributed MEMS transmission lines (DMTL's) operating up to 60 GHz. The design of the DMTL's requires an accurate knowledge of the distributed loading capacitance of the MEMS bridges, as well as the residual internal stress of the bridge material. Both of these parameters are dependent upon the fabrication process, which must be characterized very carefully before measured results can be expected to match the design.

The per unit-length capacitance C_t and inductance L_t of the unloaded CPW line, shown in Fig. 2(a), are given by [7]

$$C_t = \frac{\sqrt{\epsilon_{\text{eff}}}}{cZ_o} \quad \text{and} \quad L_t = C_t Z_o^2 \tag{1}$$

where ϵ_{eff} and Z_o are the effective dielectric constant and impedance, respectively, of the unloaded CPW line and c is the free-space velocity. If it is assumed that the MEMS bridge only loads the transmission line with a parallel capacitance C_b, then the impedance Z_l and phase velocity v_l of the loaded line, shown in Fig. 2(b), become

$$Z_l = \sqrt{\frac{L_t}{C_t + C_b/s}} \quad \text{and} \quad v_l = \frac{1}{\sqrt{L_t(C_t + C_b/s)}} \tag{2}$$

where s is the periodic spacing of the MEMS bridges and C_b/s is the distributed MEMS capacitance on the loaded line. Thus, the loaded line can be designed for $Z_l = 50\ \Omega$ by appropriately choosing an unloaded-line impedance $Z_o > 50\ \Omega$ and the periodic spacing s for a given MEMS bridge capacitance C_b. In addition to the impedance change, the phase velocity of the loaded line is decreased below that of the unloaded line. In fact, it has been observed that the phase velocity of the loaded line is slower than the phase velocity in the dielectric (for a quartz substrate). Thus, the slow-wave mode on the loaded line cannot radiate since the modes in the air and dielectric both have faster phase velocities [8].

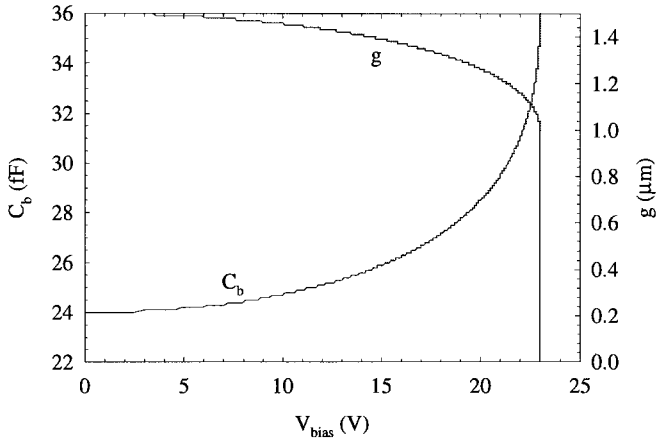


Fig. 3. Variation of the MEMS bridge capacitance and gap height with applied bias voltage for a zero-bias capacitance of 24 fF and a pull-down voltage of 23 V.

The periodic structure has an upper frequency limit due to the Bragg reflection occurring at [6]

$$f_{\text{Bragg}} = \frac{1}{\pi s\sqrt{L_t(C_t + C_b/s)}}. \tag{3}$$

In order to push the Bragg frequency above the region of interest ($f_{\text{Bragg}} \gg 60$ GHz) and maintain the loaded-line impedance at $Z_l = 50\ \Omega$, both the periodic spacing and the width of the MEMS bridge should be reduced. Another option is to increase the impedance of the unloaded line, resulting in a decrease in the per-unit length capacitance C_t. However, changing the unloaded-line impedance also affects the line loss and the pull-down voltage of the MEMS bridge. In this paper, we have chosen to keep the CPW dimensions constant ($W = G = 100\ \mu$m) with $Z_o = 96\ \Omega$, and have varied the bridge width and periodic spacing to achieve loaded lines with different Bragg frequencies. The choice of the CPW center conductor width $W = 100\ \mu$m becomes a compromise given that the total width of the line should be kept below $\lambda_d/8$ for higher order mode-free operation, and that the minimum bridge width w is 30 μm. On the one hand, it is desirable to have a pull-down voltage in the range of 10–20 V and, therefore, a wide center conductor is needed [see (6)]. On the other hand, a high unloaded impedance is needed ($Z_o = 96\ \Omega$) and, therefore, a narrow center conductor, such that the periodic spacing required to achieve a 50-Ω loaded line will result in a Bragg frequency much greater than 60 GHz. For 20–60-GHz applications, a center conductor width in the range $70 < W < 140\ \mu$m seems to be a good compromise; however, this has not been rigorously studied, and research is currently being done to optimize these tradeoffs.

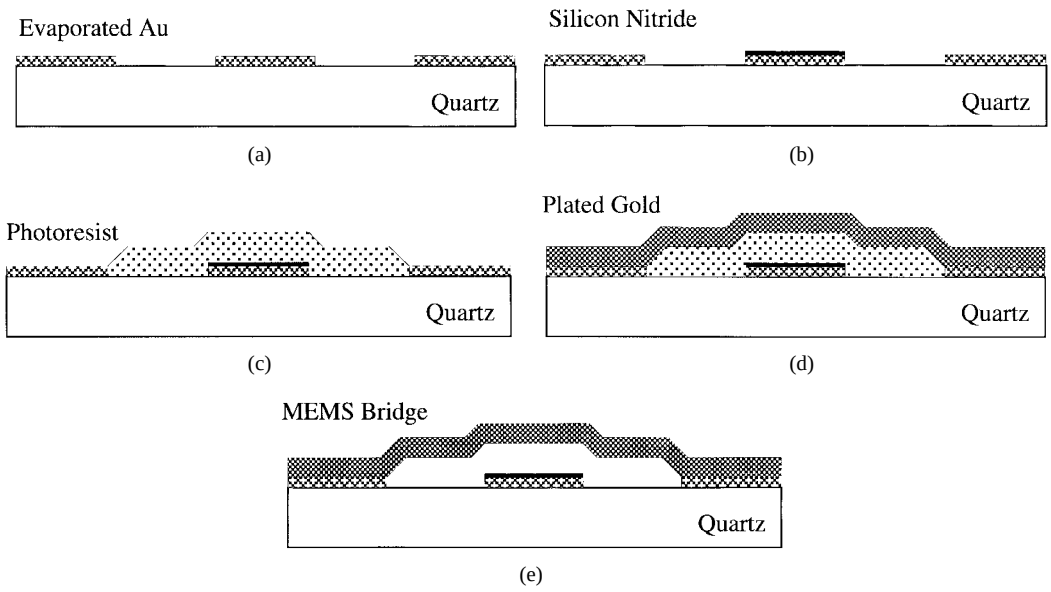


Fig. 4. Details of the fabrication process for the MEMS bridges.

The force on the MEMS bridge due to an applied bias on the CPW center conductor is given by

$$F = \frac{\epsilon_o W w}{2g^2} V_{\text{bias}}^2 \quad \text{N} \tag{4}$$

where ϵ_o is the free-space permittivity, W is the center conductor width, w is the width of the MEMS bridge, g is the bridge height, and V_{bias} is the applied bias voltage. The spring constant of the bridge is approximated by [9]

$$k = \frac{32Et^3w}{L^3} + \frac{8\,\sigma(1-\nu)tw}{L} \quad \text{N/m} \tag{5}$$

where E is the Young's modulus of the bridge material, t is the bridge thickness, $L = (W + 2G)$ is the bridge length, σ is the internal residual stress of the bridge, and ν is Poisson's ratio. The pull-down voltage of the MEMS bridge can be found by setting up a force–balance equation between the electrostatic force and the restoring force of the bridge. From the solution to this equation, it is found that the MEMS bridge becomes unstable at $2g_o/3$, where g_o is the zero-bias bridge height. The voltage at which this instability occurs is the "pull-down" voltage and is given by

$$V_p = \sqrt{\frac{8\text{k}}{27\epsilon_o W w}\, g_o^3} \quad \text{V}. \tag{6}$$

Table I gives some example calculations of the pull-down voltage of gold MEMS bridges for varying levels of stress. It is evident from these calculations that to achieve $V_p \leq 20$ V for the given dimensions, the MEMS bridge must have less than 20 MPa of stress.

Fig. 3 shows the MEMS bridge capacitance C_b versus applied bias voltage V_{bias} for the case of a zero-bias capacitance of 24 fF and a pull-down voltage of 23 V. It is seen that as the applied bias approaches the pull-down voltage, the MEMS bridge capacitance changes very rapidly and reaches 1.5 C_{bo} at 23 V, where C_{bo} is the zero-bias bridge capacitance. Because the MEMS bridge cannot be maintained at $2g_o/3$ without becoming unstable, it is not possible in practice to achieve such an increase in the MEMS bridge capacitance. Instead, the applied voltage is limited to 21–22 V, which gives a capacitance value of $C_b = 29.5$–31 fF, or a 23%–30% increase in the zero-bias bridge capacitance.

TABLE I
THE YOUNG'S MODULUS AND POISSON'S RATIO FOR GOLD ARE $E = 80$ GPa AND $\nu = 0.42$, RESPECTIVELY. THE BRIDGE DIMENSIONS USED IN THE CALCULATION ARE $g_o = 1.5$ μm, $L = 300$ μm, $W = 100$ μm

σ	V_p (t=1 μm)	V_p (t=0.5 μm)
0 MPa	10 V	4 V
20 MPa	21 V	14 V
100 MPa	43 V	30 V

B. Fabrication

The DMTL's are fabricated on a 500-μm-thick quartz substrate ($\epsilon_r = 3.8$) using finite-ground plane CPW [10]. The fabrication process is shown in Fig. 4. The CPW lines are defined first by evaporating a 500/5000-Å layer of Ti/Au [see Fig. 4(a)]. Next, a 500-Å Cr adhesion layer is sputtered over the wafer, and then a 1000-Å plasma-enhanced chemical vapor deposition (PECVD) Si_xN_y layer is grown on top. The silicon nitride is patterned with photoresist and etched in a reactive ion etching (RIE) such that it is only covering the CPW center conductor [see Fig. 4(b)]. Once the photoresist masking layer is removed, the exposed Cr is etched. Next, the sacrificial photoresist layer, which determines the height of the MEMS bridge, is patterned [see Fig. 4(c)]. The nominal height of the air bridges, above the center conductor, is 1.5 μm. A 500/2000/500-Å Ti/Au/Ti seed layer is evaporated and patterned with photoresist to define the width and periodic spacing of the MEMS bridges. The MEMS bridges and CPW ground planes are then gold-electroplated to a thickness of approximately 2.5 μm, followed by removal of the top photoresist and seed layer [see Fig 4(d)]. Thus, the MEMS bridge is a bilayer metal composed of Ti/Au since the titanium

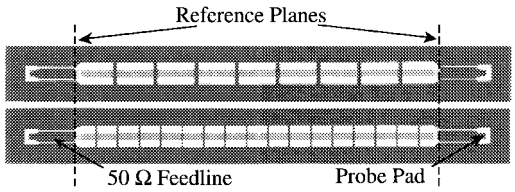


Fig. 5. Picture of fabricated DMTL's. The CPW dimensions of the loaded lines are $W = G = 100$ μm and of the feedlines are $W = 150$ μm and $G = 16$ μm. The width and spacing of the MEMS bridges are 60 μm/580 μm and 30 μm/306 μm, respectively, resulting in a total length of 5.2 mm.

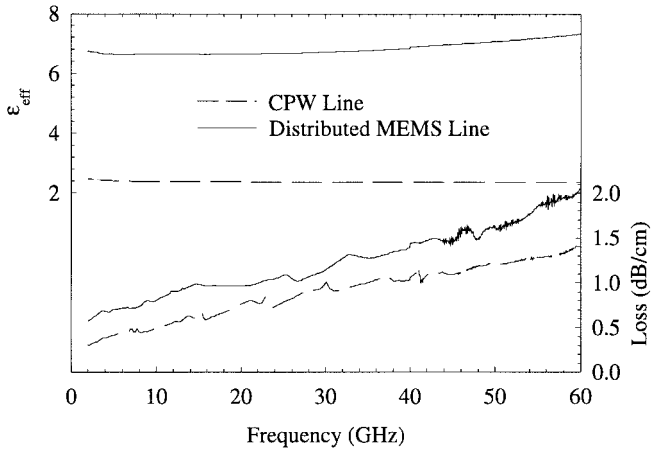


Fig. 6. Deembedded effective dielectric constant and loss from TRL calibrations of the loaded ($W = G = 100$ μm, $w = 30$ μm, $s = 306$ μm) and unloaded ($W = 150$ μm, $G = 16$ μm) CPW transmission lines.

is not removed from the bottom of the bridge. The last step is to remove the sacrificial photoresist by soaking the wafer in acetone. At this point, the wafer cannot be air dried because the surface tension of the liquid will pull the MEMS bridges down, causing them to stick to the substrate. Therefore, the wafer is placed in denatured ethanol and a critical-point drying system is used to release the MEMS bridges [see Fig. 4(e)] [11]. Fig. 5 shows a loaded CPW line connected to probe pads via 50-Ω CPW feedlines ($W = 150$ μm, $G = 16$ μm), in which the center conductors are also electroplated.

C. Measurements

Measurements of the DMTL's were taken using an HP8510C for 2–40 GHz and an HP8510C with a U-band millimeter-wave test set for 40–60 GHz. The measurements were calibrated using NIST's MultiCal[1] thru-reflection-line (TRL) calibration routine and TRL standards fabricated on-wafer. MultiCal deembeds the effective dielectric constant and loss from the measured TRL lines. Therefore, a comparison of the DMTL's with the unloaded CPW lines can be made by constructing the necessary TRL standards in both lines. The unloaded CPW lines used for this purpose are the 50-Ω feedlines ($W = 150$ μm, $G = 16$ μm) and the DMTL's used ($W = G = 100$ μm) have 30-μm-wide bridges spaced at 306 μm. Fig. 6 shows the effective dielectric constant and loss deembedded from the measurements of the CPW and DMTL calibration lines.

[1]MultiCal is a registered trademark of NIST, Boulder, CO 80303.

The measured effective dielectric constant of the unloaded CPW line has an average value of 2.37 and is nearly invariant with frequency. This value agrees very closely with the static value of 2.34 computed using the Maxwell[2] two-dimensional (2-D) static-field solver. The measured loss of the CPW line is 0.9 dB/cm at 30 GHz. In comparison, the measured effective dielectric constant of the DMTL is 6.7 from 18 to 33 GHz and slowly rises to 7.3 at 60 GHz. The measured attenuation of the DMTL is 1.3 dB/cm at 30 GHz. The increase in the attenuation of the DMTL over the unloaded CPW line is due to several competing effects. The attenuation is: 1) decreased due to a gap size of 100 μm instead of 16 μm; 2) increased due to a center conductor thickness of 0.5 μm instead of an electroplated center conductor; and 3) increased due to the presence of the distributed MEMS bridges. Nevertheless, a loss of 1.3 dB/cm at 30 GHz is acceptable for millimeter-wave applications.

Using the TRL calibration of the unloaded CPW feedlines with the reference planes, as shown in Fig. 5, DMTL's with different-width bridges and periodic spacing were measured. Fig. 7(a) shows the measured S-parameters of a line with 16 30-μm-wide MEMS bridges spaced at 306 μm (total length = 5.17 mm) with a nominal MEMS bridge height of 1.5 μm and a bridge thickness of 2.5 μm. The line impedance ($Z_l = 61$ Ω) is calculated from the first peak in $S11$, knowing that the line is behaving as a quarter-wave transformer at this frequency. The loading capacitance C_b is, therefore, calculated to be 24 fF from (2), using the static values of $Z_o = 96$ Ω and $\epsilon_{\text{eff}} = 2.37$ ($W = G = 100$ μm) to obtain L_t and C_t. This capacitance value agrees very well with the value of $C_b = 23.8$ fF found by simulating a single MEMS bridge using the Maxwell three-dimensional (3-D) static-field solver. The 23.8-fF bridge capacitance can be broken into a parallel-plate capacitance $C_{||} = \epsilon A/d = 17.7$ fF and a fringing capacitance $C_f = 6.1$ fF. It is interesting to note that the fringing capacitance is quite high and cannot be neglected in the analysis of narrow bridges. Using $C_b = 24$ fF, the calculated effective dielectric constant is 5.9, which underestimates the TRL deembedded value of 6.7. The effective dielectric constant can also be calculated using the first two sets of nulls in $S11$ and the total length of the distributed line. A value of 6.8–7.1 is obtained up to 40 GHz, which agrees well with the TRL value of 6.7. The calculated Bragg frequency of this line, using $C_b = 24$ fF, is 129 GHz. The measured loss of the distributed line agrees very well with the TRL deembedded loss (1.3 dB/cm at 30 GHz).

The measurement shown in Fig. 7(b) is of a DMTL with 16 60-μm-wide MEMS bridges spaced at 640 μm (total length = 10.8 mm). The calculated MEMS bridge capacitance from (2) is $C_b = 48$ fF, which agrees fairly well with the value obtained from the Maxwell 3-D static-field solver of $C_b = 42.5$ fF ($C_{||} = 35.4$ fF, $C_f = 7.1$ fF). The difference could be due to slight nonuniformities in the bridge height or the result of inaccuracies in the peak reflection coefficient ($S11 = -13.6$ dB) measurements and, therefore, impedance and capacitance calculations. For example, an error of ± 1 dB in the peak of $S11$ measurements results in an error

[2]Maxwell is a registered trademark of Ansoft Corporation, Pittsburgh, PA 15219.

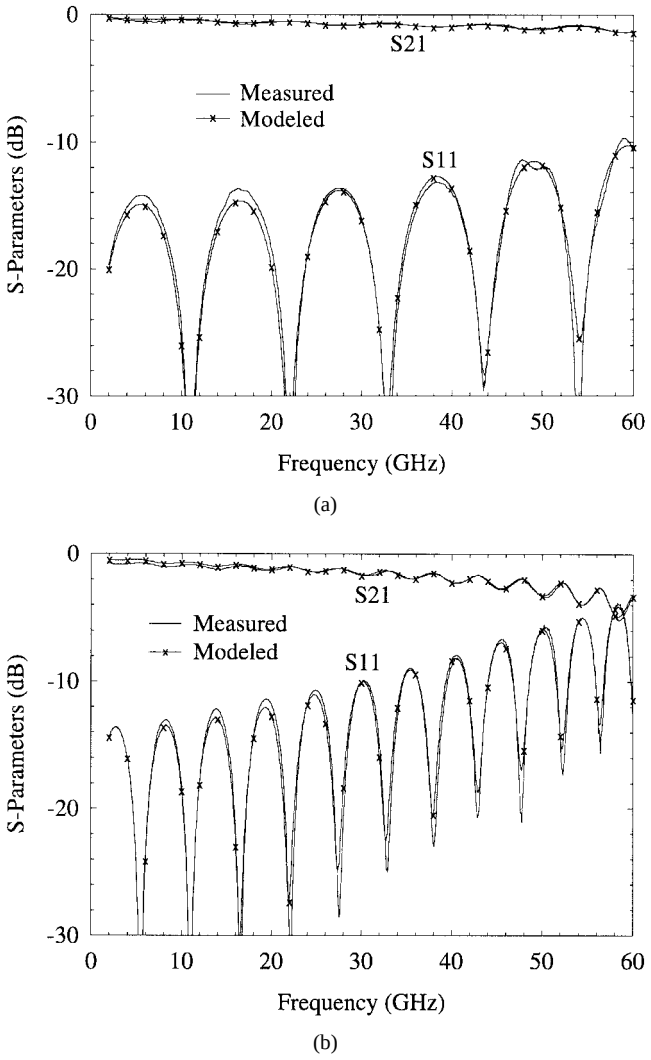


Fig. 7. Measured and simulated S-parameters of DMTL's with (a) 16 30-μm-wide MEMS bridges spaced at 306 μm (total length = 5.2 mm, $Z_l = 61\ \Omega, f_{\rm Bragg} = 129$ GHz) and (b) 16 60-μm-wide MEMS bridges spaced at 640 μm (total length = 10.8 mm, $Z_l = 62\ \Omega$, $f_{\rm Bragg} = 62$ GHz).

of $\pm 1.5\ \Omega$ and ± 4 fF for the line impedance and bridge capacitance, respectively. The calculated effective dielectric constant for $C_b = 48$ fF is 5.7, while the value obtained from the first two sets of nulls is 6.2–6.5. Although the impedance of this line is approximately the same as the first line ($\sim 62\ \Omega$), this line has a much lower Bragg frequency due to the larger loading capacitance and periodic spacing. The calculated Bragg frequency is 62 GHz, which agrees well with the measured results. Both distributed lines show that the peak of the reflection coefficient approaches -10 dB at approximately half of the Bragg frequency.

D. Modeling

In addition to the measured data plotted in Fig. 7 is the simulated data of the DMTL's calculated using the model shown in Fig. 8. In this model, the unloaded line impedance Z_o, the spacing of the MEMS bridges s, the number of periodic sections n, and the effective dielectric constant of the unloaded line $\epsilon_{\rm eff}$ are determined from the initial design. The

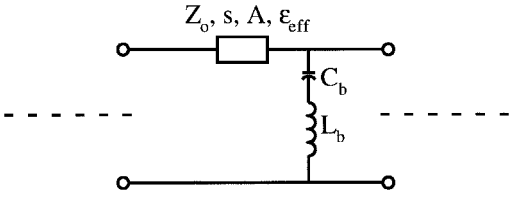


Fig. 8. Model used for a section in the DMTL simulation where Z_o is the unloaded line impedance, s is the periodic spacing of the bridges, A is the attenuation of the unloaded line, $\epsilon_{\rm eff}$ is the effective dielectric constant of the unloaded line, C_b is the bridge capacitance, and L_b is the bridge inductance.

TABLE II
COMMON PARAMETERS OF BOTH DMTL'S ARE $Z_o = 98\ \Omega$, $\epsilon_{\rm eff} = 2.37$, $n = 16$

w/s	30/306 μm	60/640 μm
C_b	25 fF	48 fF
L_b	23 pH	14 pH
A(@ 20 GHz)	0.52 dB/cm	0.6 dB/cm

unloaded line attenuation A, bridge capacitance C_b, and bridge inductance L_b are all varied to fit the model to the measured data. The model is analyzed using HP EESof's Libra,[3] in which the attenuation follows a $\sqrt{f}$ variation.

Table II lists the parameters used in the model for the 30/306-μm and 60/640-μm lines. It is seen that the fitted capacitance is very close to the value given by the 3-D static-field solver (see Section II-C). It is important to note that the unloaded-line attenuation A (0.52–0.6 dB/cm @ 20 GHz), is not the same as the measured loaded-line attenuation (see Fig. 6). The reason is that the loaded-line attenuation takes into account the multitude of standing waves on the DMTL. The effect of the standing wave on the loss of the DMTL is modeled by simulating the 16 sections together, using the unloaded-line attenuation A. The inductance in the model is essential for matching the nulls in $S11$ above 15 GHz since it contributes an increasing series reactance, which counteracts the decreasing series reactance due to the bridge capacitance. As can be seen in Fig. 7, the model fits very well with the measured data, including the Bragg effect seen in the 60/640-μm line. At low frequencies ($f < 12$ GHz), the modeled value of $S21$ is seen to underestimate the measured loss due to the additional skin effect losses, which are not taken into account in the model.

III. TTD DISTRIBUTED MEMS PHASE SHIFTER

As mentioned previously, the DMTL can be used as a TTD phase shifter. This is done by applying a single bias voltage to the center conductor of the CPW line. This applied voltage causes the height of the MEMS bridges to be decreased, thereby increasing the capacitive loading and decreasing the phase velocity. Although this analog control voltage is susceptible to noise from the power supply, the fact that only one control voltage is required is a major advantage and could be very beneficial in quasi-optical phased arrays.

[3]HP EESof Communications Design Suite v6.0, Hewlett-Packard Company, Santa Clara, CA, 1995.

A DMTL with 32 30-μm bridges spaced at 306 μm (total length = 10.1 mm) was tested as a phase shifter. The pull-down voltage for this line was measured to be 23 V, thus, the maximum voltage that could be applied without the bridges becoming unstable was 22 V. The measured phase shift and insertion loss are shown in Fig. 9(a) and (b), respectively, for varying bias voltages. From these results, it is seen that a maximum phase shift of 118° at 60 GHz is achieved with 2.1 dB of loss. Also, it should be noted that the null period of $S11$ decreases as the bias voltage is increased from 0 to 22 V. The phase shift is linear with frequency up to 40 GHz, with 1.6-dB loss and $-67°$ phase shift. It then drops at a slightly steeper slope, which is an effect of approaching the Bragg frequency of the line. In Fig. 9(b), it is seen that as the bias voltage is increased, the line impedance is lowered from 59 Ω at 0 V to 56 Ω at 22 V due to the increased capacitive loading of the line. The increased loading corresponds to an increase in the bridge capacitance from $C_b = 27$ fF at 0 V to $C_b = 31$ fF at 22 V. The calculated Bragg frequency for $C_b = 31$ fF ($V_{\text{bias}} = 22$ V) is 119 GHz. Also, it is important to note that the insertion loss of the distributed MEMS phase shifter remains nearly constant as the bias voltage (and phase shift) is varied. The phase shift per millimeter is $-6.6°$/mm at 40 GHz and $-11.7°$/mm at 60 GHz.

It should be noted that this distributed line ($w = 30$ μm, $s = 306$ μm) with 32 bridges resulted in an impedance of $Z_l = 59\ \Omega$ and $C_b = 27$ fF as compared to the 16 bridge line (same w and s) presented in Section II-C (see Fig. 7) with $Z_l = 61\ \Omega$ and $C_b = 24$ fF. This could be due to process variations in the bridge height or to errors in the measurement of the peak of $S11$, as detailed in Section II-C. However, in modeling the data, it was found that a zero-bias bridge capacitance of 28 fF and a 22-V bias capacitance of 32.6 fF was necessary to match the nulls in $S11$, as well as the phase shift. As can be seen in Fig. 9(a), the modeled phase shift at 22 V matches almost perfectly with the measured data over the entire 60-GHz bandwidth. The associated values used for this model are $L_b = 18$ pH, $A = 0.6$ dB/cm at 20 GHz, $n = 32$, and $s = 306$ μm. Using the *linearly* extrapolated value of $-98°$ at 60 GHz, the maximum time delay of this line is 4.5 ps.

Fig. 10 shows measured results for two more examples of DMTL phase shifters with $W = G = 100$ μm. The results shown in Fig. 10(a) are for a line with 16 60-μm-wide bridges spaced at 580 μm (total length = 9.8 mm). The insertion loss is 1.7 dB at 40 GHz, the reflection coefficient ranges from -15 dB to -10 dB, and the maximum phase shift is $-82°$ ($-8.4°$/mm). The time delay at 23 V, calculated from the linear phase shift (0–27 GHz), is 4.5 ps. The line has a zero-bias impedance of 60 Ω and a Bragg frequency of 67 GHz. The phase shift at 23-V bias is also modeled and, as can be seen in Fig. 10(a), the simulated results match very well with the measured data. The modeled zero-bias capacitance is 48 fF and increases to 57 fF at 23 V. The other parameters used in the model are: 1) $L_b = 16$ pH; 2) $A = 0.6$ dB/cm @ 20 GHz; 3) $n = 16$; and 4) $s = 580$ μm. The measured results shown in Fig. 10(b) are from a line fabricated on a different wafer, where the MEMS bridges are only 1-μm thick, rather than

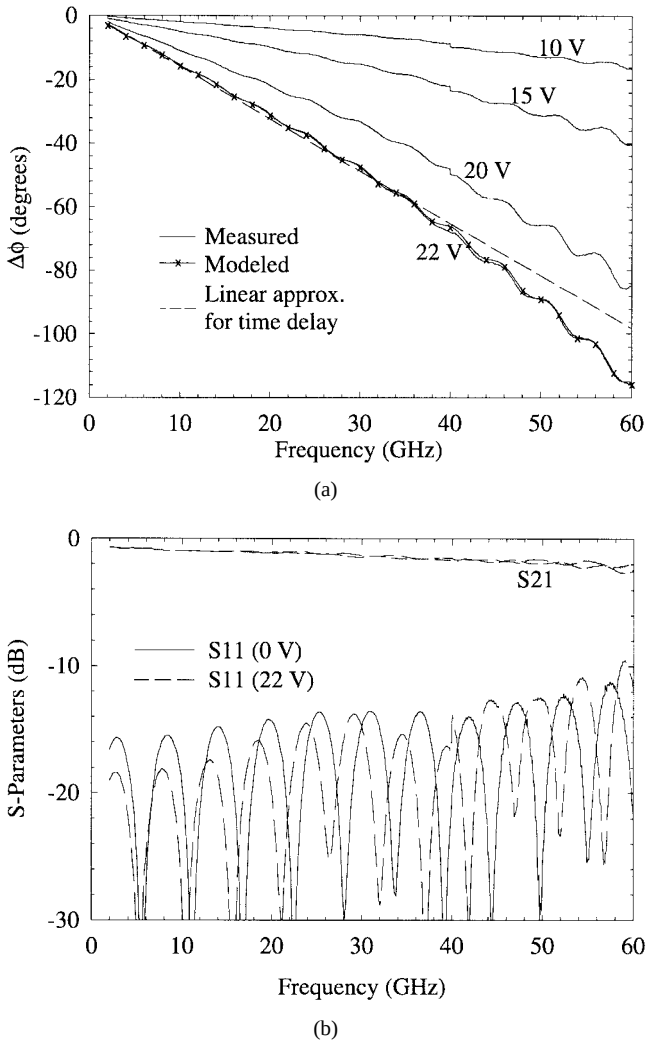
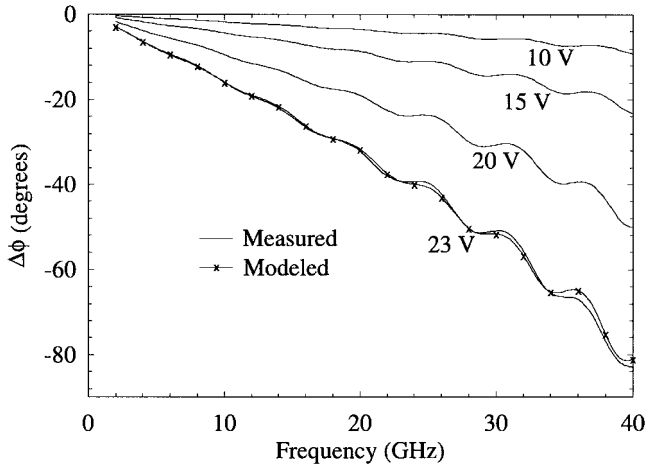


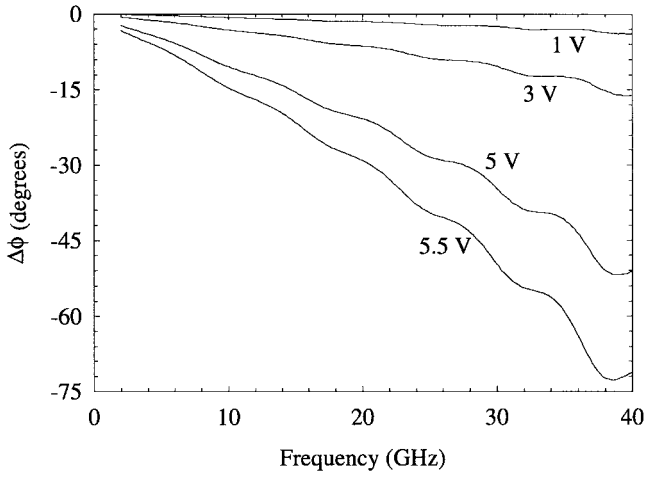
Fig. 9. Measured (a) phase shift and (b) S-parameters for a DMTL phase shifter with 32 30-μm-wide bridges spaced at 306 μm (total length = 10.1 mm) for varying bias voltage. The phase shift at 22 V is modeled with simulated results shown in (a).

2.5-μm thick, and do not have a titanium layer on the bottom. The measured pull-down voltage of the MEMS bridges for this line is 6 V (as compared to 23 V). The line is composed of 16 60-μm-wide bridges with a periodic spacing of 400 μm (total length = 6.74 mm) resulting in a zero-bias impedance of 43 Ω. The maximum phase shift of this line is seen to be $-74°$ ($-11°$/mm) and has an associated loss of 1.4 dB at 40 GHz with a reflection coefficient ranging from -16 to -11 dB. The maximum time delay from the linear phase shift (0–29 GHz) is 4.2 ps. The zero-bias MEMS bridge capacitance is calculated to be 87 fF, which is much higher than the simulated value of 42.5 fF. This, together with the low pull-down voltage ($V_p = 6$ V), indicates the presence of a fairly large compressive stress, which may have caused the bridges to buckle down slightly. The calculated Bragg frequency for $C_b = 87$ fF is 69 GHz. Another effect of the compressive stress in the bridges is that this DMTL could not be modeled successfully due to the nonuniformity in the bridge height.

It is evident from Fig. 10 that the lines with lower Bragg frequencies and lower loaded-line impedances (i.e., higher



(a)



(b)

Fig. 10. Measured phase shift versus bias voltage for DMTL phase shifters with (a) 16 60-μm-wide bridges spaced at 580 μm (total length = 9.8 mm) and (b) 16 60-μm-wide bridges spaced at 400 μm (total length = 6.7 mm). The phase shifter in (b) has a pull-down voltage of 6 V and a MEMS bridge thickness of 1 μm. The phase shift at 23 V is modeled with simulated results shown in (a).

C_b/s) result in more phase shift per millimeter in their region of operation. In fact, the line with 60-μm-wide bridges spaced at 400 μm ($Z_l = 43\ \Omega$, $f_{\text{Bragg}} = 69$ GHz) has 67% more phase shift per millimeter at 40 GHz than the line with 30-μm-wide bridges spaced at 306 μm ($Z_l = 60\ \Omega$, $f_{\text{Bragg}} = 124$ GHz). Work is currently being done to design distributed TTD phase shifters for optimal phase shift per millimeter and low insertion loss.

Fig. 11 shows the operation of the DMTL's as phase verniers at 40 GHz. The measurement was done on three lines with identical bridge widths (30 μm) and spacings (306 μm). The number of bridges on each line is labeled in the plot. As can be seen from the measurement, 12°/36°/62° phase shift at 40 GHz can be achieved over a 21-V bias control for the 8/16/32 bridge DMTL's with an associated insertion loss of 0.51/0.75/1.57 dB. Thus, very fine control of the phase (0°–12°) can be achieved with 0.5-dB insertion loss. This is well suited for applications in which a digital master clock drives several direct digital synthesizers to achieve TTD over a large array of antenna elements. A phase vernier is needed to fine tune the phase between the antenna elements.

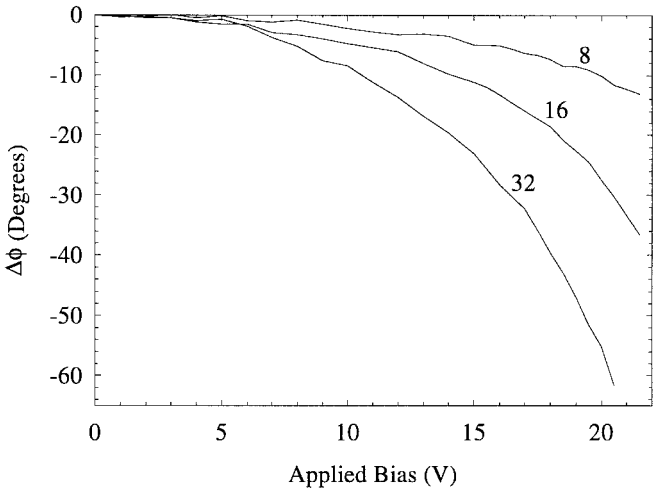


Fig. 11. DMTL lines measured as phase verniers at 40 GHz. All three lines have 30-μm-wide bridges spaced at 306 μm with the number of bridges shown in the plot. The insertion loss is 0.51/0.75/1.57 dB for the 8/16/32 bridge DMTL's.

IV. Distributed Wide-Band MEMS Switches

Millimeter-wave switches are an essential element in radar and communications systems. Typically, their function is to switch between the transmit and receive modes or to switch an antenna beam in Rotman lenses or focal-plane designs. Also, many millimeter-wave instrumentation switches in vector-network analyzers require 60–70-dB isolation. These are typically built using p-i-n diodes and have an insertion loss of -10 dB from 40 to 60 GHz. Recent results of W-band p-i-n diode switches have demonstrated 1.6-dB loss with 20-dB isolation over a 10-GHz bandwidth centered at 80 GHz [12]. The wide-band distributed MEMS switches presented in this paper only work to 60 GHz; however, it is believed that high performance can also be achieved at W-band frequencies (i.e., >40-dB isolation with <2-dB insertion loss).

The DMTL switch works by applying a bias voltage greater than the pull-down voltage. This causes the MEMS bridges to be clamped down on top of the center conductor with the 1000-Å-thick Si_xN_y layer separating them. Thus, the MEMS bridge capacitance is greatly increased and an RF short to ground is obtained above a certain frequency. The upper frequency of the distributed switch is determined by the Bragg frequency when the bridges are up. As was noted at the end of Section II-C, acceptable performance ($S11 < -10$ dB) can be obtained up to about half of the Bragg frequency.

Fig. 12 shows results for DMTL's with eight and 16 30-μm-width bridges ($t = 2.5$ μm) spaced at 306 μm (total length = 2.7 mm and 5.2 mm, respectively) resulting in a loaded impedance of 60 Ω. The Bragg frequency for these lines is 129 GHz, which limits their upper frequency of operation to approximately 65 GHz. The insertion loss, with the bridges in the up position, is 0.4/0.6 dB for eight bridges and 0.7/1.3 dB for 16 bridges at 30/60 GHz. When the bridges are pulled down with a voltage of 30–35 V ($V_p = 23$ V), the cutoff

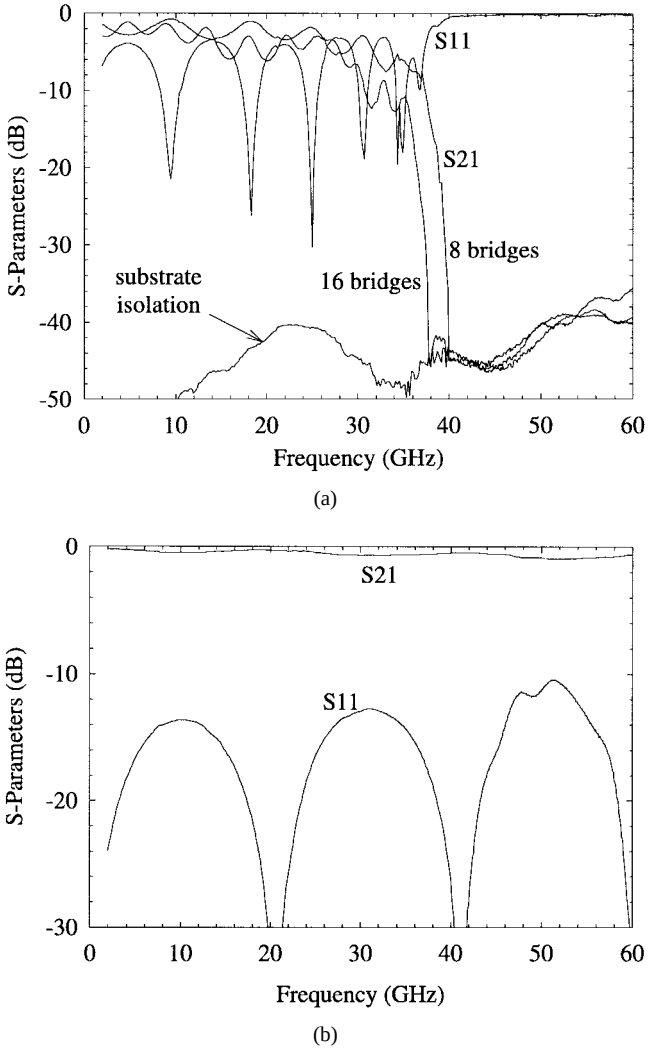


Fig. 12. Measured results of distributed MEMS switches with eight and 16 30-μm-wide bridges spaced at 306 μm in the (a) closed position (bridge down) and (b) open position. The S-parameters for the open position are only shown for the case of the eight-bridge design [S-parameters for the 16-bridge design are given in Fig. 7(a)].

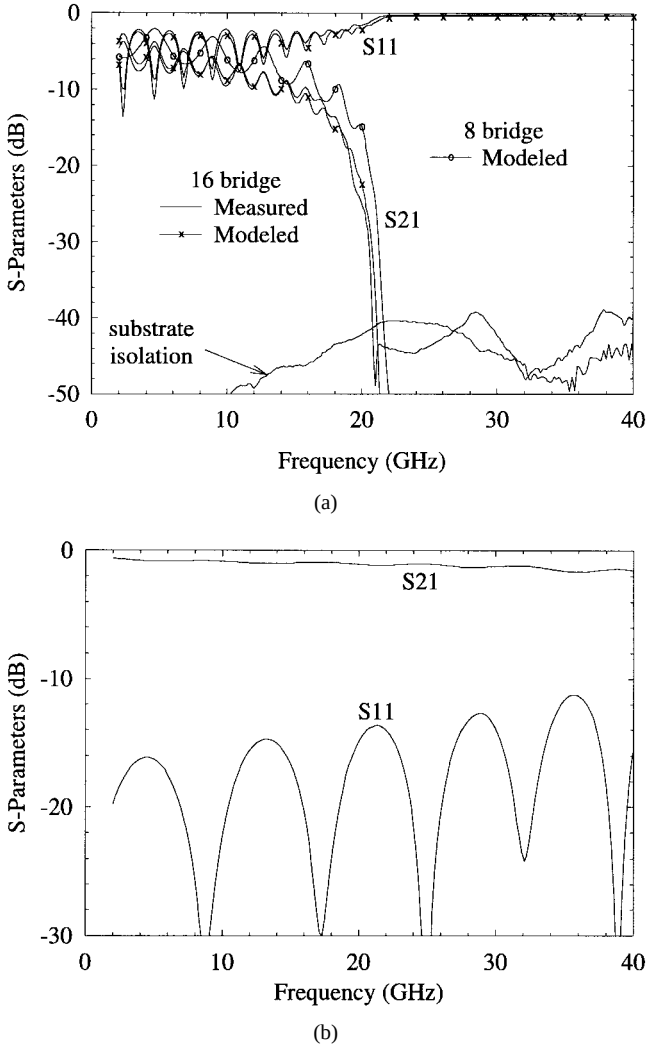


Fig. 13. Measured and modeled results for a distributed MEMS switch with 16 60-μm-wide bridges spaced at 400 μm in the (a) closed position (bridge down) and (b) open position.

frequency is 40 GHz for the eight-bridge design and 38 GHz for the 16-bridge design, giving an operational bandwidth of 40–60 GHz. The switch isolation is limited to 40–45 dB by substrate radiation of the finite ground-plane CPW lines. Notice that the eight- and 16-bridge designs result in nearly the same response.

Fig. 13 shows results for a DMTL with 16 60-μm-wide bridges spaced at 400 μm (total length $=$ 6.7 mm) resulting in an impedance of 43 Ω. The Bragg frequency is 69 GHz, which limits the upper frequency of operation to approximately 35 GHz. However, the measured S-parameters indicate that the switch can be used to 40 GHz. The insertion loss, with the bridges in the up position, is 0.9/1.4 dB at 20/40 GHz. When the bridges are pulled down with a voltage of 15–20 V ($V_p = 6$ V), the cutoff frequency is 21 GHz, which results in an operational bandwidth of 21–40 GHz.

The closed-switch results shown in Fig. 13(a) are successfully modeled using the DMTL model given in Fig. 8. The pulled-down bridge capacitance and bridge inductance are 0.9 pF and 12 pH, respectively. The transmission-line attenuation needed to fit the data is 1.1 dB/cm at 20 GHz. This is double the value used previously (see Section II-D) and is believed to be due to the additional losses of the large capacitors formed by the MEMS bridge, 1000 Å of Si_xN_y, and the CPW center conductor. Using this model, the performance of a switch with eight bridges was simulated with the results also shown in Fig. 13(a). Obviously, it is more efficient to use eight bridges since this design will result in half the insertion loss (0.5/0.7 dB at 20/40 GHz) for the same "brick-wall" response and operating bandwidth. The switch isolation is again limited by the CPW line substrate radiation.

It should be noted that the closed switch in Fig. 12 could not be modeled successfully because a high enough bias voltage could not be applied to these switches in order to obtain a uniform down capacitance in every bridge. The bias voltage is limited in this case by the breakdown voltage of the Si_xN_y, which is approximately 35 V. On the other hand, the closed switch in Fig. 13(a) had a pull-down voltage of 6 V; so an applied bias of 20 V is sufficient to obtain uniform capacitance values along the transmission line.

V. Discussions and Conclusions

This paper presents, to our knowledge, the first MEMS-based 0–60-GHz TTD phase shifters and high-isolation wide-band switches to date. The essential idea is to include the capacitance of the MEMS bridge, in the up position, as part of the transmission-line design, rather than treating it as a parasitic capacitance, as is done in current MEMS switch designs. An immediate advantage is that the MEMS bridges can be fabricated with a 1–1.5-μm height above the transmission line and, therefore, require a substantially lower pull-down voltage than current designs (10–20 V instead of 28–60 V). The TTD phase shifters offer low–loss performance and are extremely wide-band (0–60 GHz), limited only by the Bragg frequency of the loaded transmission line. The high-isolation switches are currently limited by substrate mode leakage at -45 dB, and the results indicate that eight MEMS bridges per switch is enough to obtain a "brick wall" response. The associated losses in the TTD phase shifters and the wide-band high-isolation switches are state-of-the-art and have the potential for even further improvement in subsequent designs. In addition to this, a transmission-line model has been developed, which gives excellent agreement with the measured data.

It is evident from the TTD phase-shifter measurements that in order to achieve the highest phase-shift per millimeter, one should design for the lowest possible loaded-line impedance and Bragg frequency, while keeping $S11$ below -10 dB. If a relatively narrow bandwidth (less than 20%) is required, as is the case in most radar and communication systems, then it is possible to achieve a very large phase shift per millimeter with the use of 30–35-Ω loaded lines. An excellent match can be obtained by using $\lambda/4$ impedance transformers at the input and output ports of the TTD phase shifter. Alternatively, the CPW lines could be integrated on thin dielectric membranes to reduce the effective dielectric constant (and the transmission-line capacitance) of the unloaded line and, therefore, result in a higher loading effect from the distributed MEMS bridge capacitance. This will, in turn, result in a much larger phase shift per millimeter than DMTL's on quartz substrates. It is, therefore, obvious that the design optimization of TTD phase shifters requires the consideration of both the electrical and mechanical design aspects of the problem. This optimization is currently being researched at the University of Michigan at Ann Arbor.

The performance of TTD phase-shifters/wide-band switches is not limited to 60 GHz, and MEMS-based TTD phase shifters can easily be designed up to 110 GHz and even up to 300 GHz (with reduced periods and much higher Bragg frequencies). MEMS bridges can operate well into the millimeter-wave and submillimeter-wave range because they have very low parasitic inductances and series resistances [2]. For the wide-band distributed switches, it is important to investigate the minimum number of bridges needed for a wide-band distributed-like performance. It is obvious that this number lies between two and eight bridges, and work is currently being done to evaluate this.

Finally, future work will include investigation of the mechanical aspects of the MEMS bridge designs. The residual stress in the MEMS bridges needs to be better understood so as to result in reliable and repeatable pull-down voltages. Also, the speed of the MEMS bridges will be measured. It is expected that the MEMS bridges used in the TTD phase shifters will be substantially faster than typical MEMS bridges since they need to move only 0.4 μm and not 3–4 μm. In addition, new MEMS bridge designs with minimal stress points and maximum contact area when pulled down will be investigated.

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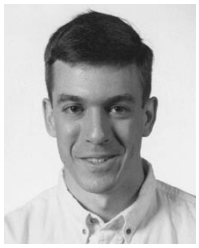

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