5–100 GHz InP Coplanar Waveguide MMIC Distributed Amplifier

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Abstract—**A single-stage 5–100 GHz InP MMIC amplifier with an average gain of more than 5.5 dB has been developed. This MMIC distributed amplifier has the highest frequency and bandwidth of operation (5–100 GHz) reported to date for wide-band amplifiers. The average associated (not optimized) noise figure of the MMIC amplifier was approximately 5.8 dB measured over 4–40 GHz. The active devices in this seven-section distributed amplifier were 0.1 μm mushroom gate, InGaAs–InAlAs lattice-matched HEMT's on a semi-insulating InP substrate. Coplanar waveguide was the transmission medium for this 100 GHz MMIC with an overall chip dimension of 500 μm by 860 μm.**

I. Introduction

MILLIMETER-WAVE systems for commercial and military applications are becoming increasingly important. Present *W*-band (75–110 GHz) radar, communication, and surveillance systems have the disadvantages of being bulky, complex, and expensive because of their waveguide and hybrid integrated circuit components [1]. Monolithic millimeter-wave integrated circuit (MMIC) technology, however, provides an alternative to conventional millimeter-wave component design and system integration, where various circuits can be monolithically integrated on a single chip. Therefore the development of these MMIC's will be the key to miniature, high-volume, low-cost, and potentially higher performance commercial and military systems at these frequencies.

We recently reported the first 94 GHz (90–100 GHz bandwidth) MMIC amplifier, which used InGaAs–InAlAs-InP HEMT's on an indium phosphide (InP) substrate [2]. Although discrete InGaAs-channel HEMT's with 94 GHz gain in hybrid amplifiers had been previously demonstrated [3], MMIC amplifiers had only been reported to frequencies below 65 GHz with less than an octave bandwidth [4]. The highest frequency multioctave MMIC distributed amplifier reported had a bandwidth of 0.5–50 GHz [5]. The highest frequency coplanar waveguide (CPW) MMIC distributed amplifier had a bandwidth of 2–18 GHz [6]. We report the results for a 5–100 GHz InP MMIC distributed amplifier with an average gain of more than 5.5 dB. Also, although 100 GHz CPW frequency-multiplier and mixer circuits have previously been reported [7]–[9], this work presents the first 100 GHz wide-band CPW circuit on an InP substrate.

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II. Device Characteristics

The active device in the MMIC was a lattice-matched $In_{0.53}Ga_{0.47}As$–$In_{0.52}Al_{0.48}As$ HEMT that was also lattice-matched to its semi-insulating InP substrate. The cross section of this device is shown in Fig. 1 (where mole fractions are as indicated). The large conduction band discontinuity between InAlAs and InGaAs [10] and the larger $\Gamma-L$ valley separation (0.55 eV) of InGaAs [11] compared with AlGaAs–GaAs make InGaAs–InAlAs more attractive for high-speed device applications. For HEMT's this material structure has the advantages of a higher sheet carrier (two-dimensional electron gas) density, higher low-field electron mobility, higher electron saturated velocity, and higher electron peak velocity. These advantages result in a higher frequency, lower noise HEMT particularly suited for millimeter-wave MMIC applications.

The material structure was grown by molecular beam epitaxy (MBE) on an iron-doped semi-insulating InP substrate. The growth temperature was 490°C, and the corresponding growth rates for both InGaAs and InAlAs were approximately 0.3 μm/h. The unintentional background doping of InGaAs was of the order of $10^{15}/cm^3$. The mole fraction of indium was 53% in InGaAs and 52% in InAlAs, resulting in a lattice-matched HEMT on InP. For this structure we have measured a sheet carrier density of more than $2.5\times10^{12}/cm^2$, and a 77 K mobility of 28000 cm^2/Vs. The undoped InGaAs layer at the top surface improved the breakdown characteristics of the device [12].

Also shown in Fig. 1 is the 0.1 μm mushroom gate of the HEMT, which is very important for its high-frequency performance. The fabrication of this gate is one of the most critical steps of the process. For the gate fabrication of these devices, a bilayer photoresist process using a copolymer layer on top of a PMMA layer was used [13].

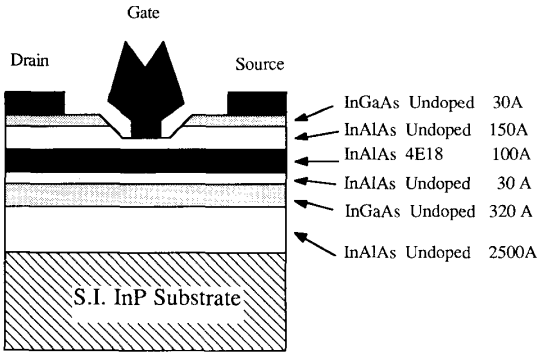

Fig. 1. Cross section of InGaAs–InAlAs–InP HEMT.

Fig. 2. SEM photograph of the 0.1 μm gate of InGaAs–InAlAs–InP HEMT.

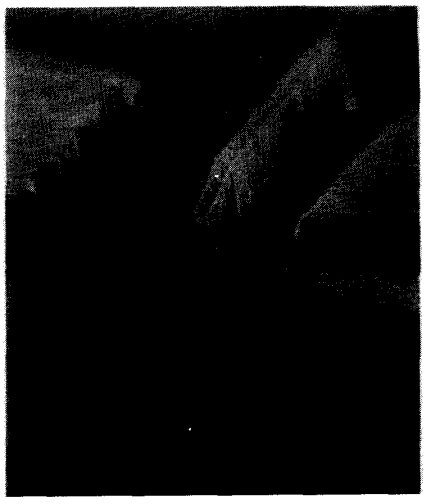

Fig. 3. SEM photograph of the device cross section of a 0.1 μm InGaAs–InAlAs–InP HEMT.

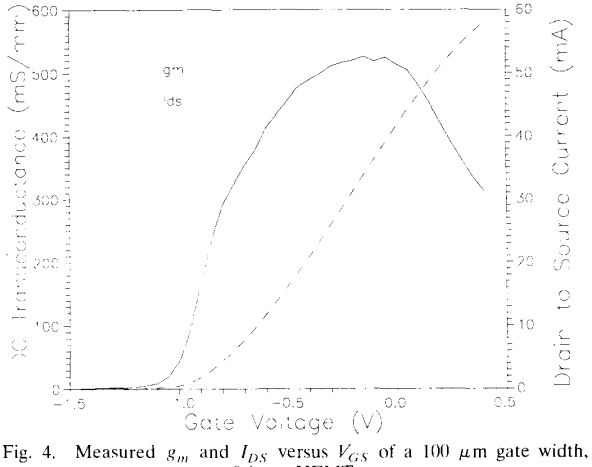

Fig. 4. Measured g_m and I_{DS} versus V_{GS} of a 100 μm gate width, 0.1 μm HEMT.

The 0.1-μm-long gate of this HEMT was defined by means of commercially available E-beam lithography. However, special care was taken in calibrating the off-axis focus, stigmation, and distortion corrections of this E-beam machine. The mushroom gate profile was used to reduce the series gate-metal resistance. The metallization was evaporated Ti–Pt–Au with a total thickness of 4000 Å. A SEM photograph of the 0.1 μm mushroom gate of the InGaAs–InAlAs HEMT is shown in Fig. 2. The source and drain ohmic contacts were standard alloyed Ni–Au–Ge metallization. Fig. 3 shows a SEM photograph of the device cross section including these source and drain contacts.

III. Device Modeling

Characterization of 0.1 μm InGaAs–InAlAs HEMT's was performed using a dedicated discrete device mask set before the MMIC's were designed. Both dc and RF parameters of devices with a wide range of gate widths were measured, and these data were used in developing device small-signal equivalent circuit models. The discrete HEMT's used for modeling had gate widths of 50, 100, and 200 μm with a two-finger T-gate structure. These device sizes were chosen so that scaling to an arbitrary gate width could be evaluated.

For each gate width group, dc measurements were performed on several devices. Fig. 4 shows a typical measured transconductance and output current of a 100 μm gate width device as a function of the gate-to-source voltage. A maximum extrinsic g_m of 540 mS/mm and a peak intrinsic g_m of approximately 650 mS/mm were obtained. The measured output current–voltage characteristics of a typical 100 μm device are shown in Fig. 5.

The 0.1 μm InGaAs–InAlAs HEMT's were also characterized at microwave and millimeter-wave frequencies, such as the one shown in Fig. 6. The S parameters of several devices with gate widths of 50, 100, and 200 μm were measured using an HP 8510B network analyzer.

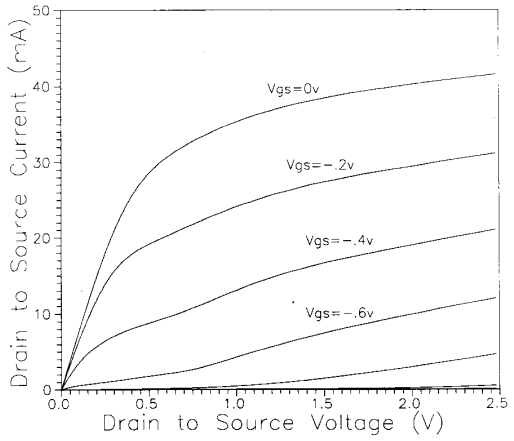

Fig. 5. Measured I_{DS} versus V_{DS} of a 100 μm gate width, 0.1 μm HEMT.

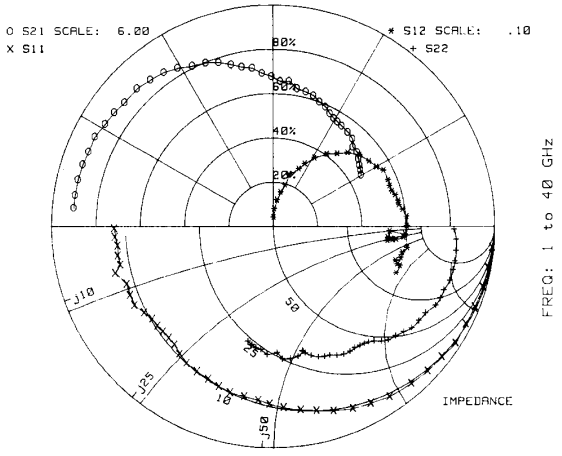

Fig. 6. Measured S parameters of a 100 μm gate width, 0.1 μm HEMT.

Small-signal equivalent circuit models were then developed from these S parameters and extracted parameter values from dc measurements for each device. Average small-signal equivalent circuit models were then developed for 50, 100, and 200 μm two-finger T-gate discrete devices. Scaling the device gate width was evaluated by comparing the small-signal equivalent circuit model of the 100 μm device with a 50 μm model scaled by 2 and a 200 μm model scaled by 1/2. Although there were differences between the models, reasonable agreement for purposes of circuit design was obtained after a few iterations of reoptimizing the equivalent-circuit models. Fig. 7 shows the equivalent circuit model of the 100 μm device which was used for the MMIC amplifier design. In this model the distributed effects of the input and output probe pads modeled as transmission lines are not shown.

We also performed experiments to investigate extrapolations of the equivalent circuit models to frequencies higher than 40 GHz. One experiment performed was to

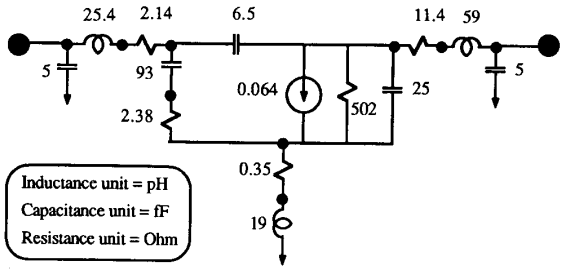

Fig. 7. Small-signal equivalent circuit model of a 100 μm gate width, 0.1 μm HEMT.

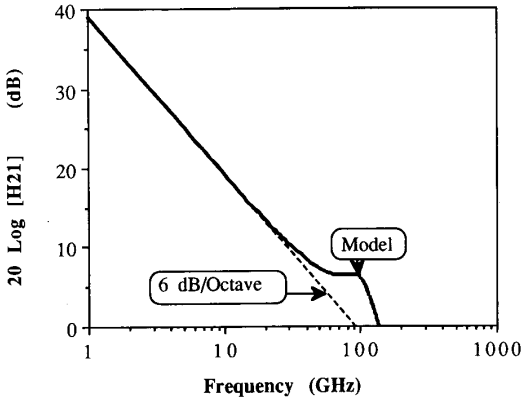

Fig. 8. Maximum current gain and F_T of a 100 μm gate width, 0.1 μm HEMT.

optimize the small-signal equivalent circuit model of a 100 μm device to measured S parameters up to 10 GHz and to compare the model and measured S parameters from 10 to 40 GHz. Although all four S parameters showed a larger phase shift from the model compared with the measured data, the most significant discrepancy in extrapolating this low-frequency equivalent circuit model to higher frequencies was in both the magnitude and phase of S_{12}. For circuit design purposes, however, the agreement between the model and the measured S parameters was adequate.

From the equivalent circuit model of the 100 μm device shown in Fig. 7, a unity-current gain (F_t) of 136 GHz and a unity-power gain frequency (F_{Max}) of 171 GHz were obtained. Current gain (H_{21}) as a function of frequency is shown in Fig. 8, and maximum power gain (MSG/MAG) as a function of frequency is shown in Fig. 9. Extrapolation of low-frequency current gain with a 6 dB/octave slope results in a unity-current gain of less than 100 GHz, as shown in Fig. 8. Extrapolating the maximum available power gain (MAG) at a slope of 6 dB/octave from the unconditional stability frequency (F_K at which the stability factor becomes greater than 1.0) results in a unity-power gain of 220 GHz. The reason for the differences between the model cutoff frequencies and the 6 dB/octave rules is the presence of the extrinsic parameters in the equivalent circuit model of the device,

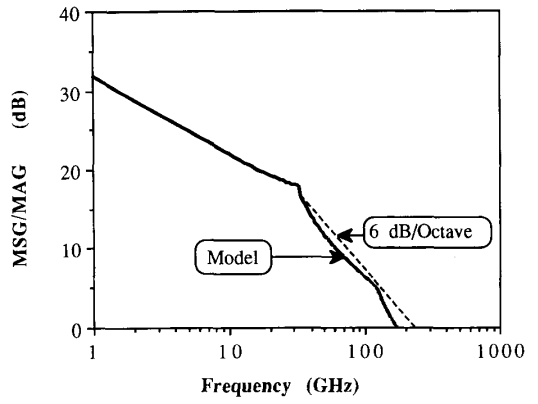

Fig. 9. Maximum power gain and F_{Max} of a 100 μm gate width, 0.1 μm HEMT.

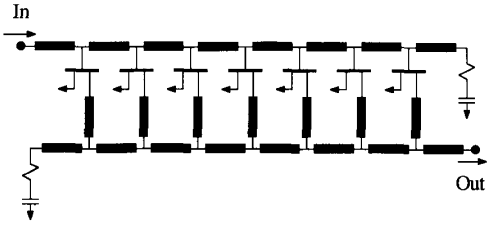

Fig. 10. Schematic circuit diagram of the seven-section distributed amplifier.

as shown in Fig. 7. Therefore F_{Max} and the extrinsic F_T are functions of these parasitic elements, some of which (such as gate–metal resistance R_G) do not exactly scale with the gate width. This caused F_{Max} and the extrinsic F_T to be slightly different for the 50, 100, and 200 μm devices which had a two-finger T-gate layout with unit finger widths of 25, 50, and 100 μm respectively. It should be noted that these characterizations and the modeling were performed on discrete devices but that the measurements of the HEMT's on the actual MMIC wafer indicated approximately 10% lower F_T and F_{Max} than the discrete HEMT's.

IV. Circuit Design

A distributed amplifier design approach was chosen for the MMIC because of its insensitivity to variations in device parameters and its equivalent circuit model. This reduced sensitivity of the circuit to device characteristics was particularly important for the 100 GHz design because of large uncertainties in the accuracy of the device equivalent circuit model at those frequencies. A schematic circuit diagram of the seven-section MMIC distributed amplifier is shown in Fig. 10. The circuit was simulated using commercially available microwave CAD programs (Touchstone of EESof Inc.). The simulation results for the gain and input/output return loss are shown in parts (a) and (b) of Fig. 11 respectively. The CPW losses as a function of frequency were also included in the transmission line model used in the circuit file. These losses,

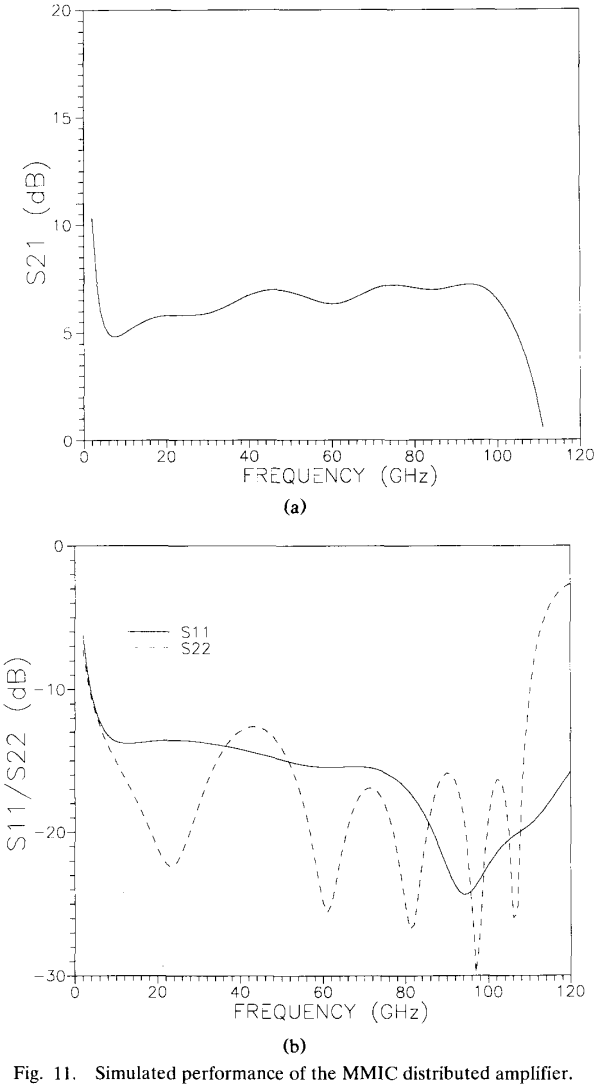

Fig. 11. Simulated performance of the MMIC distributed amplifier.

which include ohmic, dielectric, and radiation components, were obtained from measured CPW characteristics. The simulated results indicated an input return loss and an output loss of better than 10 dB up to 100 GHz, with a reasonably flat gain. Seven 0.1-μm-gate-length HEMT's with different gate widths ranging from 12 to 38 μm were used as the active devices for this amplifier. The HEMT's had an interdigitated layout with two fingers for each device. The interdigitated structure was chosen because of its compatibility with the CPW propagation medium. A scalable small-signal equivalent circuit model was used for these devices in the circuit simulation. The total gate width of all seven devices together was 166 μm.

CPW was chosen as the propagation medium for this MMIC amplifier. Compared with microstrip, a well-designed millimeter-wave CPW has the advantages of being uniplanar and of exhibiting lower dispersion, lower

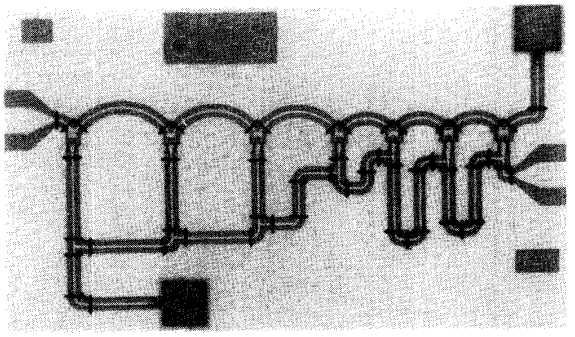

Fig. 12. Microphotograph of the fabricated MMIC amplifier.

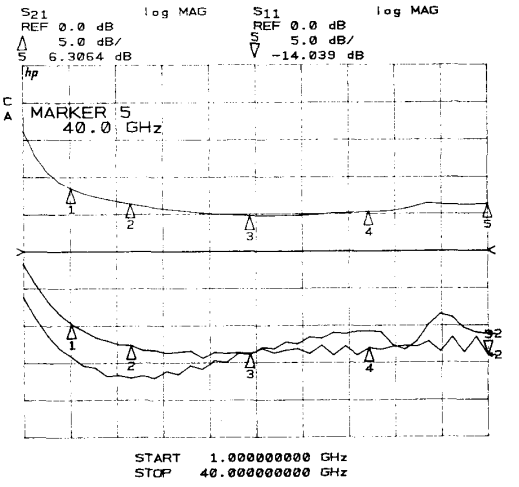

Fig. 13. Measured 1–40 GHz performance of the MMIC amplifier.

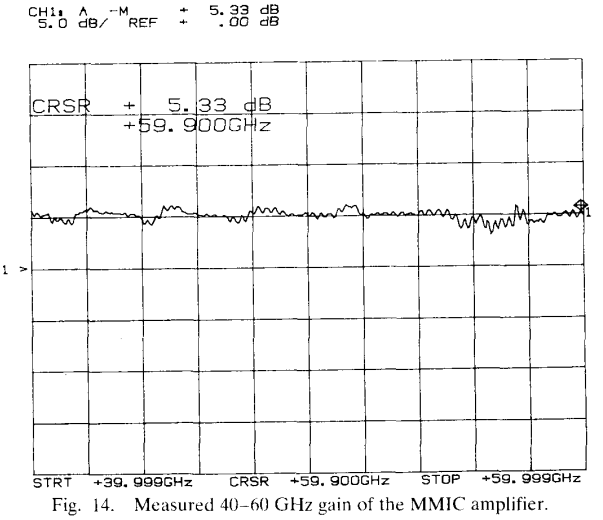

Fig. 14. Measured 40–60 GHz gain of the MMIC amplifier.

radiation losses, lower substrate thickness sensitivity, lower inductance, and easier ground plane access. One primary disadvantage of CPW, however, is its higher conduction losses. The ground-to-ground spacing of CPW determines the trade-off between its various parameters, such as dispersion, losses, and substrate thickness sensitivity. The CPW's in the MMIC amplifier were modeled by ideal lossy transmission lines for simulation. The loss factor for the CPW's was estimated from the insertion loss measurements on 50 Ω CPW's. The layout of the MMIC was such that it attempted to minimize the number of discontinuities. Microstrip discontinuity models with a microstrip substrate thickness of the order of the CPW ground-to-ground spacing were used in the simulation circuit file to approximate the CPW discontinuities.

In addition to HEMT's and CPW's, the MMIC distributed amplifier had two thin-film resistors for the terminations of its gate and drain transmission lines, and two parallel-plate capacitors. The thin-film resistors were made of sputtered TaN, and a 2000-Å-thick SiO_2 layer was used as the dielectric material for the parallel-plate capacitors. Air bridges were used to connect the two CPW ground planes for suppression of the undesired CPW even mode. These air bridges were primarily placed at the discontinuities. Standard processing techniques were used for the fabrication of the MMIC wafer. The overall chip dimensions were 500 μm by 860 μm. Fig. 12 shows a microphotograph of the fabricated InP MMIC distributed amplifier.

V. Measurement Results

The MMIC distributed amplifier was characterized from 1 to 110 GHz. An HP 8510 vector network analyzer was used to make on-wafer S-parameter measurements from 1 to 40 GHz. Fig. 13 shows the measured 1–40 GHz gain and input/output return loss of the MMIC amplifier. Scalar network analyzers were used to make on-wafer gain measurements of the same MMIC amplifier over 40–60 GHz, 60–75 GHz and 75–110 GHz ranges. Fig. 14 shows the measured gain over the 40–60 GHz frequency band and Fig. 15 shows the measured gain over the 75–100 GHz frequency band. Although the MMIC amplifier had gain up to 110 GHz, because the uncertainties associated with the accuracy of our measurements rapidly increased above 105 GHz, the gain measurement above this frequency was not considered reliable and therefore it is not shown. It should be mentioned, however, that the simulated results also indicated the amplifier had gain up to 110 GHz. Fig. 16 shows the composite data from different frequency bands for the measured gain in the InP MMIC distributed amplifier from 5 to 100 GHz. The average gain was more than 5.5 dB from 5 to 100 GHz. This MMIC amplifier actually has gain down to very low frequencies; however the return loss becomes less than 10 dB at frequencies below 5 GHz. The MMIC amplifier was dc biased for maximum gain with a drain-to-source voltage (V_{DS}) of 2.5 V, a gate-to-source voltage (V_{GS}) of 0 V, and a corresponding drain-to-source current (I_{DS}) of approximately 65 mA.

Although this MMIC distributed amplifier was not designed for optimum low-noise performance, we also mea-

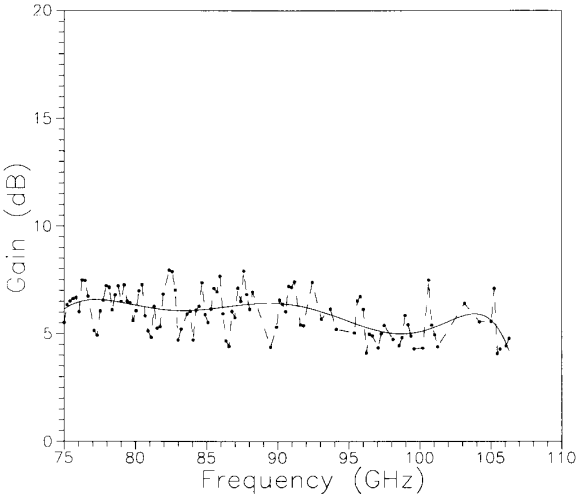

Fig. 15. Measured 75–100 GHz gain of the MMIC amplifier.

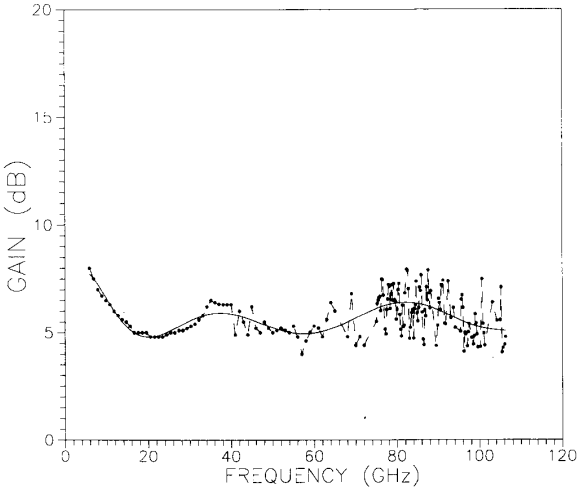

Fig. 16. Measured 1–100 GHz gain of the MMIC amplifier.

sured its noise figure. The on-wafer noise figure measurements were made using Cascade CPW probes and commercially available instruments. Fig. 17 shows the 4–40 GHz associated noise figure of the MMIC amplifier at the maximum gain bias point described. The average associated noise figure over this frequency band was approximately 5.8 dB. Although at present we could not measure the noise figure above 40 GHz because of the frequency limitations of our instruments (from our experience with other lower frequency broad-band distributed amplifiers) it is expected that the noise figure will remain relatively constant up to the cutoff frequency of the distributed amplifier, which is in excess of 110 GHz. It should also be noted that the noise figure results presented are not the minimum noise figure of the MMIC amplifier; this will be further optimized in our future measurements.

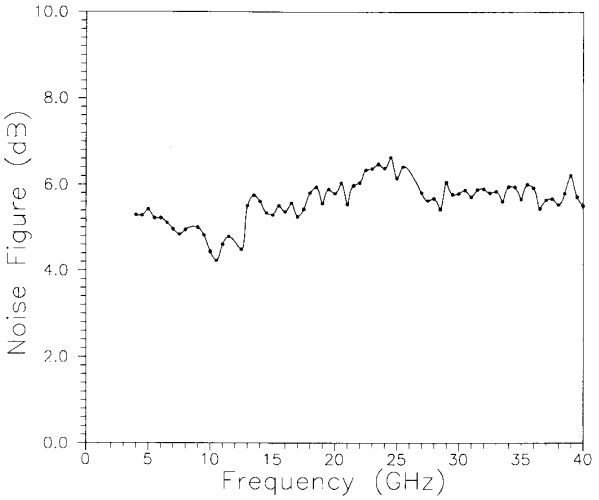

Fig. 17. Measured 4–40 GHz noise figure of the MMIC amplifier.

VI. Conclusions

We have reported a single-stage 5–100 GHz InP MMIC amplifier with an average gain of more than 5.5 dB. This MMIC distributed amplifier has the highest frequency and bandwidth of operation (5–100 GHz) reported to date for wide-band amplifiers. This MMIC amplifier had an associated (not optimized) average noise figure of 5.8 dB measured from 4.0 to 40.0 GHz, which was relatively independent of frequency. The active devices in this seven-section distributed amplifier were 0.1 μm mushroom gate, InGaAs–InAlAs lattice-matched HEMT's on a semi-insulating InP substrate. Coplanar waveguide was the transmission medium for this 100 GHz MMIC with an overall chip dimension of 500 μm by 860 μm. This work also demonstrates the application of CPW circuits for 100 GHz MMIC's.

Acknowledgment

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References

[1] G. L. Lan, J. C. Chen, C. K. Pao, M. I. Herman, and R. E. Neidart, "A *W*-band channelized monolithic receiver," in *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symp. Dig.*, 1989, pp. 95–100.

[2] R. Majidi-Ahy *et al.*, "94 GHz InP MMIC five-section distributed amplifier," *Electron. Lett.*, vol. 26, no. 2, pp. 91–92, Jan. 1990.

[3] K. H. G. Duh *et al.*, "High-performance InP-based HEMT millimeter-wave low-noise amplifiers," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1989, pp. 805–808.

[4] M. Aust *et al.*, "A family of InGaAs/AlGaAs *V*-band monolithic HEMT LNA's," in *GaAs IC Symp. Dig.*, 1989, pp. 95–98.

[5] J. Perdomo, M. Mierzwinski, H. Kondoh, C. Li, and T. Taylor, "A monolithic 0.5 to 50 GHz MODFET distributed amplifier with 6 dB gain," in *GaAs IC Symp. Dig.*, 1989, pp. 91–94.

[6] M. Riaziat, I. Zubeck, S. Bandy, and G. Zdasiuk, "Coplanar waveguides used in 2–18 GHz distributed amplifier," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1986, pp. 337–338.

[7] R. Majidi-Ahy, M. Shakouri, and D. M. Bloom, "100 GHz active electronic probe for on-wafer *S*-parameter measurements," *Electron. Lett.*, vol. 25, no. 13, pp. 828–830, 1989.
[8] R. Majidi-Ahy and D. M. Bloom, "Millimeter-wave active probe frequency-multiplier for on-wafer characterization of GaAs devices and IC's," *Electron. Lett.*, vol. 25, no. 1, pp. 6–8, 1989.
[9] R. Majidi-Ahy and D. M. Bloom, "120 GHz active wafer probes for picosecond device measurements," in *Picosecond Electronics and Optoelectronics Conf. Proc.*, 1989, pp. 31–35.
[10] D. F. Weslch, G. W. Wicks, and L. F. Eastman, "Calculation of the conduction band discontinuity for InAlAs/InGaAs heterojunction," *J. Appl. Phys.*, vol. 55, no. 8, p. 3176, 1984.
[11] K. Y. Chen, A. Y. Cho, S. G. Christman, T. P. Pearsall, and J. E. Rowe, "Measurement of the $\Gamma-L$ separation in InGaAs by ultraviolet photoemission," *Appl. Phys. Lett.*, vol. 40, p. 423, 1980.
[12] Y. C. Pao *et al.*, "Impact of surface layer on InAlAs/InGaAs/InP high electron mobility transistors," *IEEE Electron Device Lett.*, vol. 11, no. 7, pp. 312–314, 1990.
[13] M. Riaziat *et al.*, "Highest current gain cutoff frequency with 0.08 μm gate HEMT on InP," in *InP and Related Materials Proc.*, 1990, to be published.

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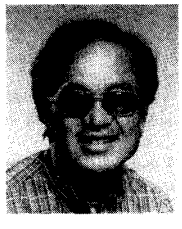

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Majid Riaziat (M'84) received the B.S. degree in engineering physics from the University of Oklahoma in 1978 and the M.S. and Ph.D. degrees in applied physics from Stanford University in 1980 and 1983 respectively.

He has been with Varian Research Center since 1984. Currently he is manager of the electro-optics group at the Varian Research Center, Palo Alto, CA. The major emphasis of this group is on the development of microwave fiber-optic networks. His previous work was with the MMIC group at Varian, where he was responsible for the development of coplanar waveguide integrated circuits as well as InP-based HEMT's, and MMIC's.

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Michael Glenn received the B.S.E.E. in 1980 from the University of Washington, Seattle, and the M.S.E.E. in 1986 from the University of Santa Clara, Santa Clara, CA.

Employed by Wiltron Company from 1980 to 1985 as a Development Engineer for their Microwave Network Analyzer Group, he was involved in circuit design for microwave test instrumentation. Working for Avantek from 1985 to 1987, he developed computer-aided test systems primarily for the measurement of power and gain compression of microwave power devices and modules. Currently he is part of the Varian Research Center's MMIC group, Palo Alto, CA, where he is involved in computer-aided measurement and characterization of microwave and millimeter-wave devices and circuits.

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S. Silverman, photograph and biography not available at the time of publication.

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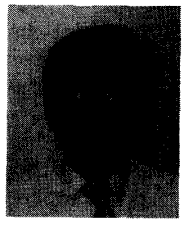

Shang-Lin Weng (M'89) received the Ph.D. degree in surface physics from the University of Pennsylvania in 1978. He was born in Taiwan in 1949 and received the B.S. degree in 1971 from the Physics Department of National Taiwan University.

In 1978 he joined Bell Laboratories (Murray Hill, NJ) as a Postdoctoral Member of Technical Staff to study surface science. In 1979 he went on to Brookhaven National Laboratory to continue his research in surface physics as a Staff Physicist. In 1983 he joined the Varian Research Center as a Senior Engineer to study molecular beam epitaxy (MBE) of III–V compound semiconductors and its application in microwave devices and circuits. In January 1990 he joined Varian MBE Equipment Operations as the Applications Lab Manager and has since been in charge of all research activities related to the advancement of MBE materials, equipment development, and marketing support.

Dr. Weng received the Wayne. B. Nottingham Prize in 1977 for his work in surface physics. He has published more than 35 papers in a variety of refereed journals and has received one patent. He is currently

a member of the American Physical Society, the American Vacuum Society, and the Materials Research Society.

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Yi-Ching Pao (S'82–M'82) received the B.S. degree in electrophysics from National Chiao-Tung University in 1981 and the M.S.E.E. degree from Pennsylvania State University in 1983. His major studies were in the area of solid-state theory and device physics.

In 1983, he joined Varian Associates, III–V Device Center, Santa Clara, CA, where he is currently engineering manager of the MBE operation and low-noise HEMT program. His research has dealt with the development of GaAs/AlGaAs and InAlAs/InGaAs/InP processes, MBE material growth, and high electron mobility transistor designs.

Mr. Pao has authored or coauthored more than 35 papers in the fields of MBE and high-speed devices. He is currently working toward the Ph.D. degree at Stanford University under the honors co-op program. He is a member of Sigma Xi.

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George A. Zdasiuk (S'79–M'81) received the B.Sc. degree in engineering science and the M.Sc. degree in physics from the University of Toronto in 1974 and 1975, respectively. He subsequently received the Ph.D. degree in applied physics from Stanford University in 1981. His thesis research was in the area of quantum electronics.

In 1980, he joined the Varian Associates Solid State Laboratory. He has been involved in the development of submicron GaAs FET devices, microwave characterization techniques, and the design and fabrication of GaAs monolithic microwave integrated circuits. Currently, he is Associate Director of the Solid State Device Laboratory at the Varian Research Center.

Dr. Zdasiuk is a member of the American Physical Society.

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Steve G. Bandy received the B.S. degree in electrical engineering from Walla Walla College in 1965 and the Ph.D. degree in electrical engineering from Stanford University in 1970.

He joined the Varian Research Center of Varian Associates in Palo Alto, CA, in 1969 and has since been responsible for advanced studies on III–V discrete FET's for use in low-noise and power applications. In 1975, he was appointed manager of the Microwave Device Group, and in 1985 he became manager of the Microwave Circuits and Devices Group of the Research Center.

Dr. Bandy is a member of Sigma Xi.

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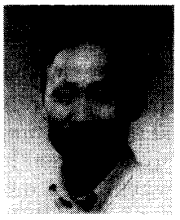

Zoilo C. H. Tan received the B.S. degree in chemical engineering from Cheng Kung University, Taiwan, in 1963, the M.S. degree in physical chemistry from the University of Arkansas in 1966, and the Ph.D. degree in nuclear chemistry from the Massachusetts Institute of Technology in 1969.

His research interests are in the development of resist and processes for advanced microlithography. He was the key inventor of Kodak MX 771 X-ray resist and ZX 784 e-beam resist. Following a brief career as staff scientist at Synertek Inc., he joined the Gate Array Division of Fairchild Semiconductor in 1985, where he was engaged in various resist processes for both optical and e-beam lithography. He is currently Manager of the E-Beam Center, Varian Research Center, Varian Associates, Inc., Palo Alto, CA.