# GaAs-Monolithic IC's for an X-Band PLL-Stabilized Local Source

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*Abstract* — *X*-band GaAs-monolithic voltage controlled-oscillator (VCO), divide-by-four analog frequency divider, and Wilkinson power splitter have been developed for frequency stabilization of an *X*-band local source in a phase-locked loop (PLL) system. The VCO has a series feedback configuration and utilizes an optimized design procedure to yield the highest dc-RF efficiency ever reported for a GaAs-monolithic FET oscillator. The frequency divider has a novel structure which applies a dual-gate FET mixer and two RC-coupled FET amplifier stages to establish a closed loop for generating a $\frac{1}{4}$ subharmonic component of an input frequency. The Wilkinson power splitter consists of an isolation resistor and two quarter-wavelength lines, which have been realized in both meander and spiral forms.

A VCO-driven frequency divider system incorporating these IC's consumes 380-mW total power to provide the $\frac{1}{4}$ subharmonic component of the VCO frequency with more than 3-dBm output power over a 10.86–11.01-GHz range.

## I. Introduction

With the advent of microwave direct satellite-broadcasting (DSB), increasing demand for *X*-band stable local sources has become more evident [1], [2]. To obtain such a source, current approaches make use of a dielectric resonator stabilized oscillator [1]–[4]. This method, however, suffers from problems like difficulties in monolithic integration of the whole circuit, including the dielectronic resonator, which is desirable for system mass production.

As an approach capable of meeting the above requirement, we have considered a PLL configuration, shown in Fig. 1, to realize an electronically frequency stabilized *X*-band monolithic source. In the present configuration, using a power splitter, a part of an *X*-band VCO power is coupled to a $\frac{1}{4}$ analog frequency divider to provide an *S* band signal. Then using a prescaler, the frequency of this signal is furthermore divided down to a range that can be compared with a crystal oscillator frequency, to produce a dc voltage that is applied to the VCO. Under this circumstance, if the VCO frequency is deviated from a prescribed value, the dc voltage resulted will accordingly adjust the VCO frequency to restore its previous value and, thus, stabilization can be achieved. This paper describes the design considerations, process technology, and microwave performance of the GaAs-monolithic VCO, analog-frequency divider, and power splitter in the PLL system, newly developed for realization of an 11-GHz band stable local source for DSB applications.

Manuscript received October 2, 1985; revised December 6, 1985.

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IEEE Log Number 8607976.

## II. Circuit Design

### A. VCO

An equivalent circuit for the 11-GHz band VCO developed is shown in Fig. 2. The VCO is an FET oscillator with a series feedback configuration. Such a configuration features easier integratability over a parallel feedback configuration which requires crossover of dc and RF circuits. In Fig. 2, reactance *Xg* and capacitance *Cs* are responsible for the realization of an optimum large signal negative resistance at the drain terminal corresponding to available power of the device at 11 GHz. On the other hand, the matching circuit elements are for delivery of this power to a 50-Ω load. To design *Xg*, *Cs*, and the matching elements, we have proceeded in the following manner.

Measured small-signal *S*-parameters for a discrete FET were applied to the determination of the element values in an equivalent circuit, shown in Fig. 3, which represents the FET in the oscillator circuit. Presuming that oscillator impedance varies primarily due to nonlinearity of drain resistance $R_o$, a mathematical model [5] represented in (1) was applied to formulate this nonlinearity

$$I_d = I_{dss}(1 - V_g/V_p)^2 \tanh\left[aV_d/(V_g - V_p)\right]. \quad (1)$$

The model actually simulates static characteristics for an FET, where $I_d$ and $V_d$ are, respectively, drain current and voltage, $V_g$ is gate voltage, $V_p$ is gate pinchoff voltage, $I_{dss}$ is drain saturation current, and $a$ is a fitting parameter. Fig. 4 compares the experimental $I$–$V$ curves for a 1 $\mu$m × 280 $\mu$m FET having $I_{dss} = 76$ mA and $V_p = -3.2$ V with the theoretical curves estimated employing (1), where $a = 1.9$.

Drain instantaneous voltage and current can be, respectively, written as

$$V_d = V_{ds} + v\cos\omega t$$
$$I_d = I_{ds} + i\cos\omega t$$

where $V_{ds}$ and $I_{ds}$ are drain dc voltage and current, and $v$ and $i$ are amplitudes of the signal frequency component of drain voltage and current. Applying Taylor's series expansion of (1) in the vicinity of a dc point $(V_{ds}, I_{ds})$ and equating the signal frequency component terms, one ob-

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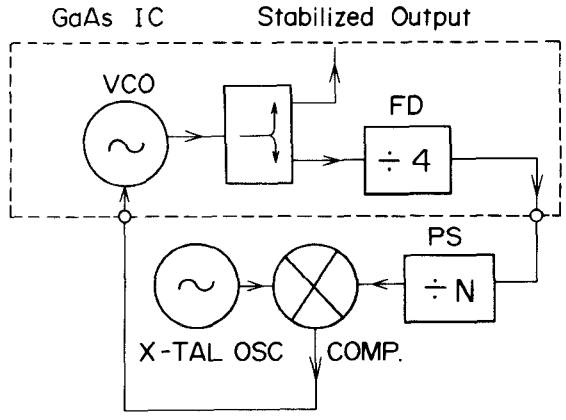



Fig. 1. Frequency stabilization in a PLL system. FD: frequency divider; PS: prescaler; COMP: comparator.

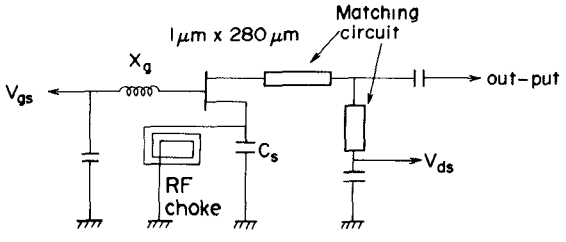



Fig. 2. An equivalent circuit for monolithic VCO.

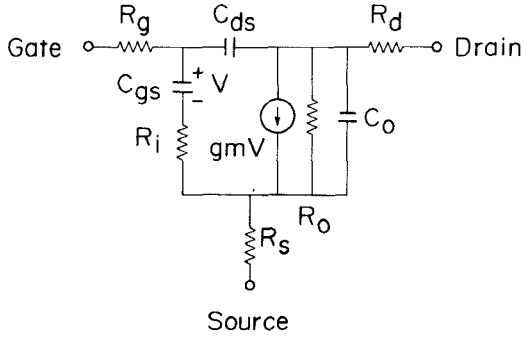



Fig. 3. An equivalent circuit representing the FET in the VCO shown in Fig. 2.

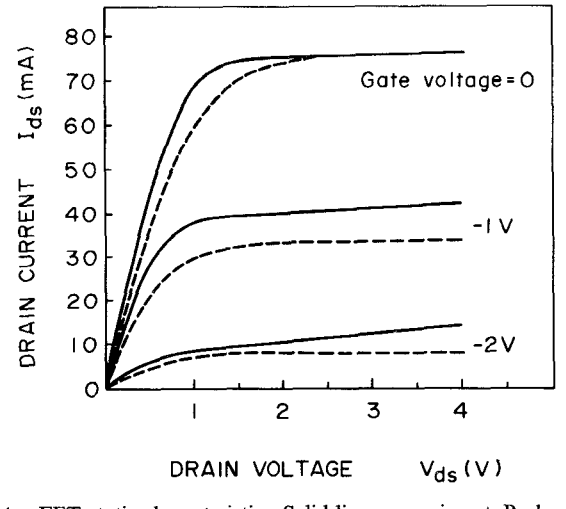



Fig. 4. FET static characteristics. Solid lines: experiment. Broken lines: theory.

tains

$$i = AB(v + CB^2v^3) \tag{2}$$

with

$$A = I_{dss}\left(1 - \frac{Vg}{V_p}\right)^2 \Big/ \cosh^2(BV_{ds})$$

$$B = \frac{a}{V_g - V_p}$$

$$C = 0.25\left[-1 + 3\tanh^2(BV_{ds})\right]$$

where interest has been restricted to the signal frequency and the effects of the higher harmonic components on the circuit operation have been ignored. Defining the drain resistance as

$$R_o = \frac{v}{i}\bigg|_{V_g = \text{const}} \tag{3}$$

and applying (2), this resistance as a function of the amplitude of drain RF current can be approximately given by

$$R_o(i) = \frac{R'_o}{1 + \beta i^{2/3}} \tag{4a}$$

where

$$R'_o = \frac{\partial V_{ds}}{\partial I_{ds}}\bigg|_{V_g = \text{const}} = \frac{1}{AB} \tag{4b}$$

represents the small-signal ($i = 0$) drain resistance and $\beta = (CB^2R'^2_o)^{1/3}$. Using (4), oscillator large-signal impedance $Z_{\text{osc}}$—the impedance seen when looking toward the FET at the drain terminal in Fig. 2—was calculated in terms of $Xg, Cs, R_o(i)$, and constant elements of the FET equivalent circuit

$$Z_{\text{osc}} = R_{\text{osc}}(Xg, Cs, R_o, \cdots) + jX_{\text{osc}}(Xg, Cs, R_o, \cdots). \tag{5}$$

Oscillation condition and output power of the oscillator are, respectively, given by

$$Z_{\text{osc}} + Z_{\text{load}} = 0 \tag{6}$$

$$P = \tfrac{1}{2}|R_{\text{osc}}|i^2 \tag{7}$$

where $Z_{\text{load}} = R_{\text{load}} + jX_{\text{load}}$ is the load impedance seen when looking toward the output at the drain terminal in Fig. 2. Considering (5)–(7), a CAD program was employed to optimize $Xg$, $Cs$, and $i$, in order to make $R_{\text{osc}}$ negative and $P$ maximum. Finally, applying (6), $Z_{\text{load}}$ and thus the matching element values were determined.

To take into account effects of simplifications and approximations made in the analysis, prior to fabricating the 11-GHz band monolithic VCO, the above design method was applied to construction of several $X$–$Ku$ band hybrid IC (HIC) oscillators, and the oscillator circuit parameters were further-optimized practically. Initial design values as well as optimum experimental values for the case of a 12-GHz band HIC oscillator using the FET of Fig. 4

TABLE I
INITIAL DESIGN VALUES AND OPTIMUM EXPERIMENTAL VALUES FOR THE CIRCUIT PARAMETERS OF A 12-GHz BAND HIC OSCILLATOR

| CIRCUIT PARAMETER | INITIAL DESIGN VALUE | OPTIMUM EXPERIMENTAL VALUE |
|---|---|---|
| $X_g$(ohm) | 30 | 20 |
| $C_s$(pF) | 0.12 | 0.14 |
| $R_{load}$(ohm) | 46 | 60 |
| $X_{load}$(ohm) | 50 | 50 |
| P(mW) | 48 | 40 |
| f(GHz) | 12 | 12.3 |

(threshold voltage $V_T = -2.5$ V, $I_{dss} = 270$ mA/mm, $g_{mo} = 130$ ms/mm) are presented in Table I.

Based on the results obtained, it was then concluded that $Xg = 20\ \Omega$, $Cs = 0.26$ pF, $R_{load} = 42\ \Omega$, and $X_{load} = 55\ \Omega$ would be required for optimum operation of an 11-GHz band GaAs-monolithic FET ($1\ \mu m \times 280\ \mu m$) oscillator.

### B. Double-Output VCO and Wilkinson Power Splitter

As we explained in Fig. 1, it is necessary to split the VCO output power for driving the $\frac{1}{4}$ analog frequency divider. For this purpose, we have designed a Wilkinson power splitter and also a VCO which inherently has two output ports.

To design the double-output VCO, the output load to the VCO was assumed to be a parallel combination of two 50-Ω impedances. Then to satisfy oscillation condition (6), the matching element values were modified accordingly. Such an oscillator can provide equal power at each output port when terminated in 50-Ω loads.

The Wilkinson power splitter, on the other hand, applies two 70-Ω quarter-wavelength transmission lines and a 100-Ω isolation resistor. Such a circuit has theoretically a usable bandwidth of 1.44:1 for an input VSWR $< 1.22$ and output port isolation $> 20$ dB under lossless conditions.

### C. $\frac{1}{4}$ Analog Frequency Divider

An equivalent circuit for the 11-GHz band $\frac{1}{4}$ analog frequency divider developed is illustrated in Fig. 5. As we explain later, the developed structure has, in general, the capability of accomplishing $1/N$ $(N = 2, 3, 4, \cdots)$ frequency division. The analog frequency divider essentially utilizes transmission lines $T_1, T_2$ for input impedance-matching, and a dual-gate FET (DGFET) mixer [6], two RC-coupled FET ($SGFET_1, SGFET_2$) amplifiers and transmission lines $T_3, T_4$ for constituting a closed-loop circuit configuration with mixing, low-pass filtering and amplification capabilities. Upon applying an input frequency $f_i$, the loop can generate two frequencies, $f_1$ and $f_2$, given by

$$f_i = f_1 + f_2 \qquad (f_1 \leq f_2) \tag{8}$$

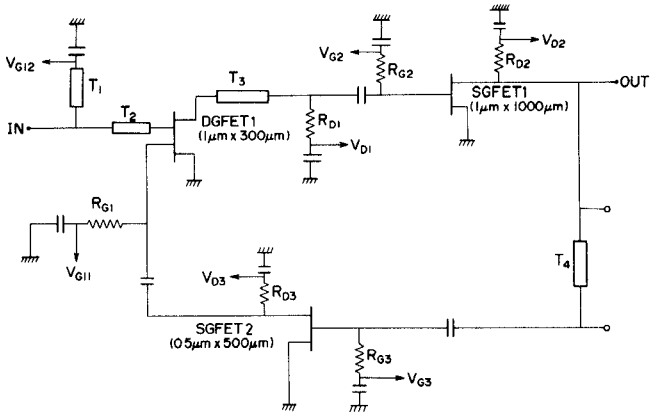



Fig. 5. An equivalent circuit for monolithic $\frac{1}{4}$ analog frequency divider.

where $f_1$ and $f_2$ satisfy a harmonic relation [7], [8]

$$f_2 = Mf_1 \qquad (M = 1, 2, 3, \cdots). \tag{9}$$

Combining (8) and (9), one thus can write

$$f_1 = \frac{f_i}{1+M} \equiv \frac{f_i}{N} \tag{10a}$$

$$f_2 = \frac{(N-1)f_i}{N} \tag{10b}$$

which implies that $1/N$ frequency division can result. For the case of $\frac{1}{4}$ frequency division, therefore

$$f_1 = \frac{f_i}{4}$$

$$f_2 = 3f_1 = \frac{3f_i}{4}.$$

To realize (10), $f_1$ requires to be in the vicinity of the natural frequency of the closed loop—a frequency at which the loop circuit has the potential to oscillate when an input signal is present. This lets frequency $f_1$ be pumped steadily in the loop with an adequately large loop gain. As a result, the pumped $f_1$ generates $f_2$, and $f_2$ in turn reproduces $f_1$ once per two loop-cycles when mixed with input frequency $f_i$. To prevent the loop from oscillating at spurious frequencies, except $f_1$ and $f_2$, other higher harmonic components, including $f_i$, are suppressed in the loop by making use of inherent low-pass filtering behavior of the RC-coupled amplifiers.

Once $f_i$ and, thus, $f_1$ are given, the closed-loop natural frequency can be accordingly designed by approximating each FET in the loop as an inverter and then applying a ring oscillation concept. Computer simulation results, obtained for the performance of the circuit shown in Fig. 5, represent that the $\frac{1}{4}$ frequency divider has a loop natural frequency equal to 2.656 GHz, and a maximum conversion gain of $-3$ dB over 8.5–10.6 GHz. Details of the computer simulation are presented elsewhere [9].

## III. FABRICATION PROCESS

Cr-doped HB GaAs substrates were used for fabricating the monolithic IC's described. Active layers for FET's and resistive layers were formed by selective $Si^+$ implantation.

An FET has a closely spaced electrode structure [10]. A single-gate FET in the oscillator chip has a 1 $\mu$m$\times$280 $\mu$m gate. In the divider chip, the gate size for DGFET is 0.5 $\mu$m$\times$300 $\mu$m, for SGFET1 is 1 $\mu$m$\times$1000 $\mu$m and for SGFET2 is 0.5 $\mu$m$\times$500 $\mu$m. A resistive layer in the Wilkinson power splitter chip has a sheet resistivity of 130 $\Omega/\square$. Observed $g_{mo}$, $V_T$, and $I_{dss}$ for an FET are 150 ms/mm, $-1.0$ V, and 120 mA/mm, respectively. Capacitors are MIM type. FET gate metal and capacitor first-level metal is Al. Transmission lines, bonding pads, and capacitor top plates are Ti/Pt/Au and Au-plated.

## IV. Microwave Performance

This section describes the RF performances for the VCO, power splitter, and frequency divider chips fabricated.

### A. VCO's

Figs. 6 and 7, respectively, show the single- and double-output VCO chip photographs. The chip size is 1.4 mm$\times$1.3 mm$\times$150 $\mu$m for the single-output VCO, and 1.8 mm$\times$1.3 mm$\times$150 $\mu$m for the double-output VCO.

The single-output VCO chip was mounted on a chip carrier and tested in a 50-$\Omega$ system. VCO performance versus variation in both drain voltage $V_{ds}$ and gate voltage $V_{gs}$ are represented in Figs. 8 and 9, respectively. Oscillation started at a drain voltage around 1.0 V and output power $P$ could reach 30 mW at $V_{ds} = 4.5$ V, $V_{gs} = -0.5$ V. DC-RF efficiency $\eta$ could take a peak value of 28 percent of $V_{ds} = 2$ V and could remain higher than 24 percent for larger voltages. We believe the value obtained for efficiency is state-of-the-art data for a GaAs-monolithic FET oscillator. While output power and efficiency were almost constant with the gate voltage $V_{gs}$, frequency of oscillation $f$ could be linearly adjusted with this voltage. Resultant pushing figure was $-400$ MHz/V.

Terminating both RF ports ① and ② of the double-output VCO in 50-$\Omega$ loads, similar experiments were carried out to test the oscillator microwave performance. Maximum output power of 11 and 13 mW could be measured at ports ① and ②, respectively, with a dc-RF efficiency equal to 21 percent, over a 10.5–10.85-GHz bandwidth. Pushing figure for the double-output VCO was $-370$ MHz/V.

Neither spurious oscillation nor frequency jumping was observed under any bias conditions for the VCO's. Results obtained for the single- as well as double-output VCO have verified validity of the design method applied.

### B. Wilkinson Power Splitter

Fig. 10 represents the fabricated power splitter chip photograph. To reduce a chip size, the quarter-wavelength segments have been realized using meander (Fig. 10(a)) and spiral (Fig. 10(b)) transmission lines. The chip size for both configurations is 1.0 mm$\times$1.3 mm$\times$150 $\mu$m. The meander-type splitter, tested in a 50-$\Omega$ system, has demon-

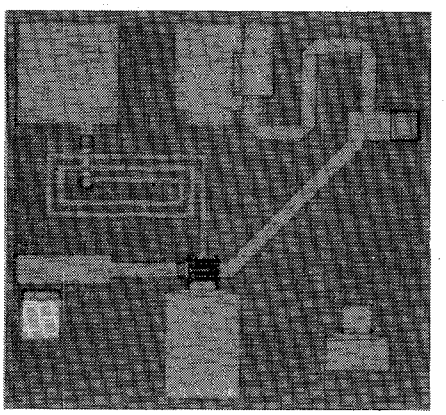


Fig. 6. A monolithic single-output VCO chip photograph.

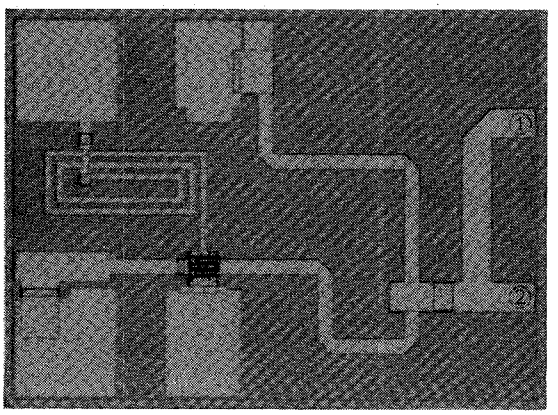



Fig. 7. A monolithic double-output VCO chip photograph.

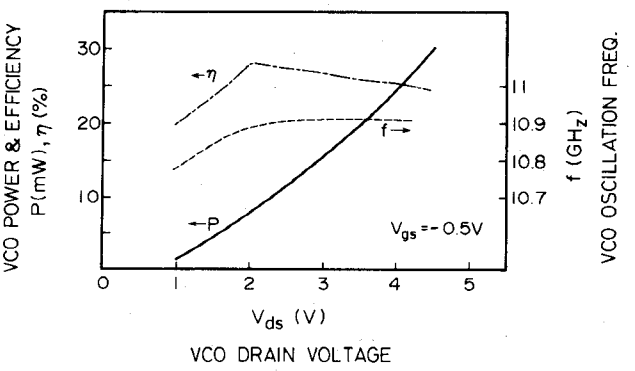



Fig. 8. Single-output VCO performance versus drain voltage.

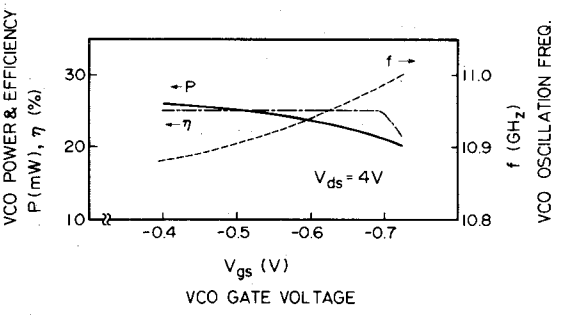
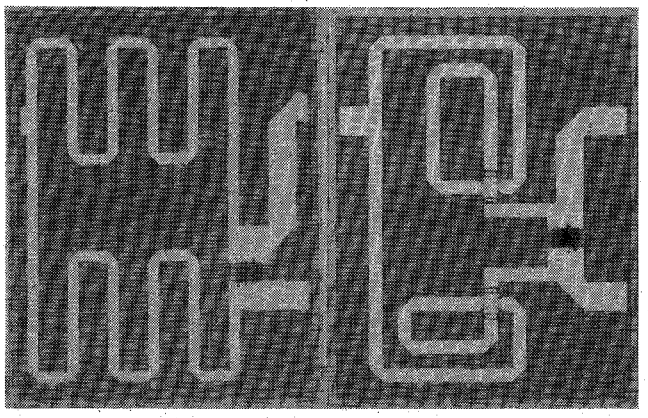



Fig. 9. Single-output VCO performance versus gate voltage.



(a) (b)

Fig. 10. Wilkinson power splitters realized using (a) meander lies, (b) spiral lines.

strated

| | |
|---|---|
| input VSWR | 1.2–1.9 |
| output port isolation | 16.5–20.3 dB |
| insertion loss | 3.9–4.2 dB |

over an 8–10-GHz range. The spiral-type splitter, on the other hand, has given

| | |
|---|---|
| input VSWR | 1.2–1.9 |
| output port isolation | 14–16.3 dB |
| insertion loss | 5–5.5 dB |

over the same frequency range. The power splitters have been designed to operate at a center frequency of 10.8 GHz. The discrepancy observed between the theory and experiment is considered to have been caused by induction of a mutual coupling between each two adjacent segments of the meander and spiral transmission lines, which has changed the effective wavelength of each line [11]. By slight modification of each line's length, however, desired characteristics can be achieved from the above chips.

The Wilkinson power splitter, which possesses an output-port isolation typically better than 15 dB, is beneficial when impedances presented to its ports are poorly matched. On the other hand, the double-output VCO exhibits no appreciable isolation among its output ports, but can successfully operate so long as the impedances connected to its ports are reasonably matched. Therefore, with relatively matched impedances, application of the double-output VCO would considerably reduce the total area occupied in a monolithic PLL system.

### C. $\frac{1}{4}$ Analog Frequency Divider

A chip photograph for the $\frac{1}{4}$ frequency divider is shown in Fig. 11. The chip size measures 1.8 mm × 1.3 mm × 150 $\mu$m. Performance for the frequency divider was investigated in a 50-Ω system. The loop natural frequency measured is 2.35 GHz. In the first experiment, an incident 10- ($=f_i$) GHZ CW signal was applied, which resulted in 2.5- ($=f_1$) GHz, 5- ($=2f_1$) GHz, and 7.5- ($=f_2$) GHz output signals. Measured output power levels for the 2.5- and 5-GHz components as a function of input drive level are

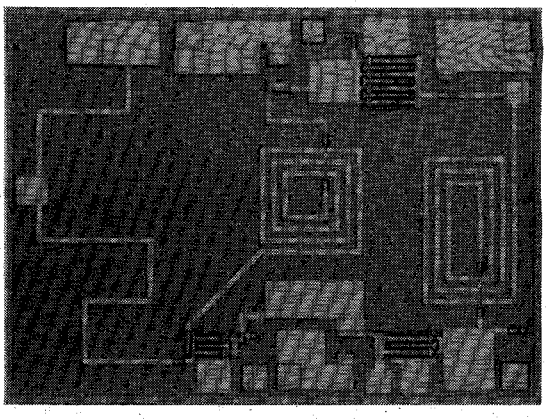


Fig. 11. A monolithic $\frac{1}{4}$ frequency divider chip photograph.

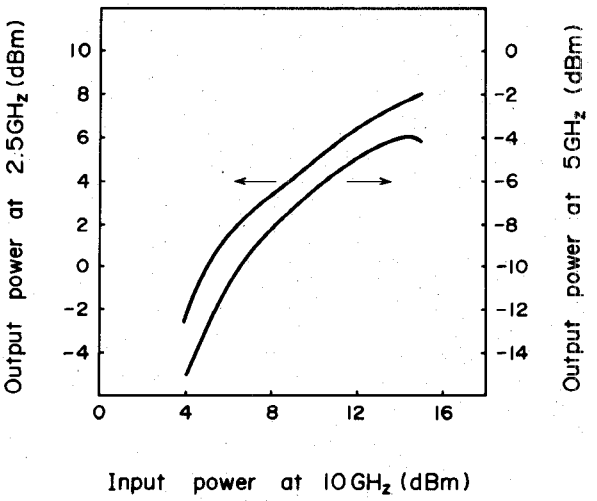



Fig. 12. Measured 2.5- and 5-GHz subharmonic output power for the frequency divider as a function of 10-GHz input drive level.

shown in Fig. 12. From the figure, the $\frac{1}{4}$ frequency signal, i.e., 2.5-GHz signal, has a maximum conversion gain of −5 dB at 10-dBm input power. Conversion gains measured for 5-GHz signal and 7.5-GHz signal (not shown in the figure) are respectively, 12 dB and 23 dB below the gain for 2.5-GHz signal. The divider was stable for a less than 3-dBm input power, and could perform $\frac{1}{4}$ frequency division over 8.5–10.2 GHz upon applying only 10-dBm input power.

To shift up the dynamic frequency range for the divider, a capacitive stub tuner was used in parallel with the output load. By doing this, the loop natural frequency was shifted up to 2.73 GHz. The externally tuned divider had no output for less than 6-dBm input. With input larger than 7 dBm, the output built up. Maximum conversion gain for the $\frac{1}{4}$ frequency component was −8 dB. Turn-on threshold response for the externally tuned divider, as a function of input frequency, is shown in Fig. 13. With a 15-dBm input power, the divider could operate at over a 10.65–11.2-GHz range.

Experimental values for natural frequency, operating bandwidth, and conversion gain for the divider are in good agreement with those estimated by computer simulation.

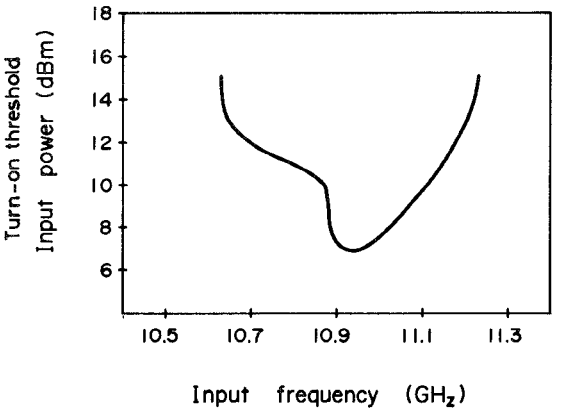



Fig. 13. Turn-on threshold response for the externally tuned frequency divider as a function of input frequency.

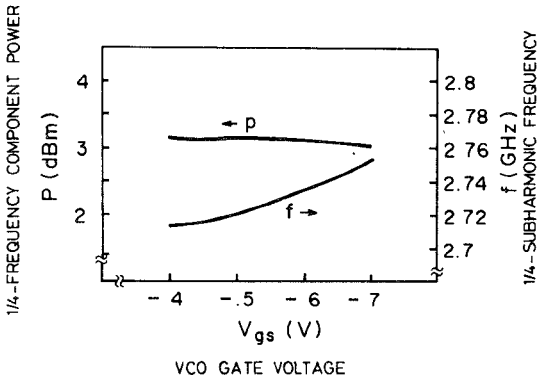



Fig. 14. Subharmonic frequency and corresponding power for the VCO-driven frequency divider versus gate voltage of driving VCO.

## V. VCO-Driven Frequency Divider Performance

In a preliminary experiment to test the performance of a unit incorporating both the VCO and frequency divider, a single-output VCO providing 14-dBm output power and the externally tuned frequency divider were employed. Using a 3-dB coupler, a part of the VCO power (11 dBm) was coupled to the frequency divider, and the VCO oscillation frequency was changed over 10.86–11.01-GHz range by adjusting the gate voltage $V_{gs}$. Under these circumstances, the system could successfully generate the $\frac{1}{4}$ frequency component of the VCO oscillation frequency with a conversion gain of about $-8$ dB. The $\frac{1}{4}$ subharmonic frequency and its power level measured, versus the VCO gate voltage $V_{gs}$, are shown in Fig. 14. To get an idea about the overall dc-RF efficiency of the system, VCO drain voltage $V_{ds}$ was changed and the $\frac{1}{4}$ subharmonic frequency power level was measured. Both the overall efficiency $\eta_t$, defined as

$$\eta_t = \frac{\frac{1}{4}\text{-subharmonic frequency power level}}{\text{dc power dissipated by VCO and frequency divider}} \times 100 \text{ percent}$$

and the $\frac{1}{4}$ subharmonic frequency power level are plotted in Fig. 15. Results obtained are in an acceptable range for driving the prescaler in the PLL system described in Fig. 1.

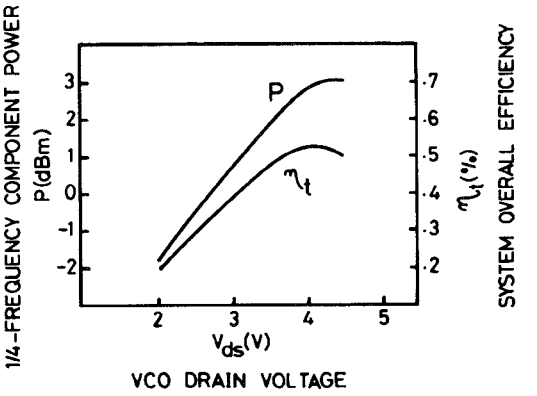



Fig. 15. Subharmonic frequency power and overall efficiency for the VCO-driven frequency divider versus drain voltage of driving VCO.

## VI. Conclusion

Design consideration and performances for $X$-band GaAs-monolithic IC's, developed for the realization of a fully monolithic stable 11-GHz band source, were described. Due to application of an optimized design procedure for the VCO, maximum dc-RF efficiency of 28 percent could be obtained, which represents the state-of-the-art data. The frequency divider has a novel structure, which permits realization of any frequency division. A VCO-driven frequency divider unit consumes 380-mW total dc power to successfully provide the $\frac{1}{4}$ subharmonic component of the VCO frequency with more than 3-dBm output power and 0.53 overall efficiency over a 10.86–11.01-GHz range.

## Acknowledgment

The authors would like to thank T. Ozawa for ion implantation and Y. Kusagai for technical assistance. Recognition is due to Y. Oi for kindly typing the manuscript. The authors also would like to thank Y. Takayama for his constant encouragement during this work.

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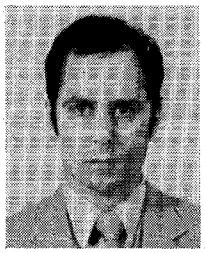

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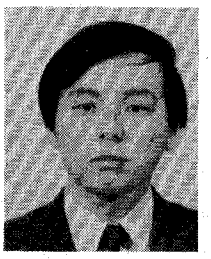

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