ment of Prof. T. Arakawa and Prof. S. Iijima at the University of Electro-Communications is gratefully acknowledged. Thanks are also due to K. Nishio for preparing the manuscript.

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2–20-GHz GaAs Traveling-Wave Amplifier

YALÇIN AYASLI, MEMBER, IEEE LEONARD D. REYNOLDS, JR., JAMES L. VORHAUS, AND LARRY K. HANES

Abstract—**Single-stage and two-stage GaAs traveling-wave amplifiers operating with flat gain responses in the 2–20-GHz frequency range are described. The circuits are realized in monolithic form on a 0.1-mm GaAs substrate with 50-Ω input and output lines. Complete gate and drain dc bias circuitry is included on the chip. By cascading these amplifier chips, a 30-dB gain in the 2–20-GHz range is demonstrated, with 9±1-dB noise figure.**

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I. INTRODUCTION

IN DISTRIBUTED OR traveling-wave amplifiers, the input and output capacitances of electron tubes or transistors are combined with inductors to form two lumped-element artificial transmission lines. These lines are coupled by the transconductance of the active devices [1]–[4].

In this work, we describe one-stage and two-stage traveling-wave amplifiers which operate in the 2–20-GHz frequency range [5]. The amplifiers are truly distributed; the gate and drain lines are two microstrip transmission lines loaded periodically by GaAs FET cells. The basic

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structure and fundamental design considerations have been reported previously [4]. In this work, the effects of gate and drain bias circuitry are also included in the design considerations.

II. Amplifier Design Considerations

A simplified schematic model for the traveling-wave amplifier gain stage is shown in Fig. 1. In this amplifier, microstrip lines periodically loaded with the complex gate and drain impedances of the FET's form lossy transmission-line structures of different characteristic impedance and propagation constants. The resultant effective input and output propagation structures, which will be referred to as the gate and drain lines, can be modelled as in Fig. 2. In this first-order analysis, the effect of the drain–gate feedback capacitance is neglected.

Approximating the gate and drain lines as continuous structures, a gain expression for the traveling-wave amplifier with n cells can be derived as follows [4]:

$$G = \frac{g_m^2 Z_0^2}{4} \frac{\left[\exp(-\alpha_g l_g n) - \exp(-\alpha_d l_d n)\right]^2}{(\alpha_g l_g - \alpha_d l_d)^2}. \quad (1)$$

This expression shows that the gain per stage of traveling-wave amplifiers does not monotonically increase with frequency. In fact, once the upper frequency of operation is determined, there exists an optimum value for n, and therefore for the total gate periphery, that can be effectively employed in a single-stage design. This maximum usable gate periphery and the maximum gain that can be expected from a single-stage amplifier is determined by the parameters of the discrete FET to be used in each cell, given the maximum frequency of operation.

We have built the amplifiers around 150-μm gate periphery devices and determined that the four-cell structure represents the optimum design for covering the 2–20-GHz band, predicting a 5.5-dB small-signal gain per stage.

The RF voltage distribution along the gate line at 20 GHz is shown in Fig. 3. Note that the RF voltage falls to 64 percent of the input voltage at the third and fourth FET's. Adding a fifth FET, therefore, does not contribute to the gain at the high end of the band. Comparison of actual calculated gains for the four- and five-cell designs in Fig. 4 illustrates this point clearly. Although the five-cell design has about 1-dB higher gain at low frequencies, it cannot maintain that gain at the high end. Hence, we believe that for the 0.8-μm vicinity gate length 150-μm FET's used in the design, the optimum use of FET periphery calls for four cells, resulting in 600 μm of total gate periphery per 5.5-dB gain stage.

Another problem that has to be addressed in determining the limits of the upper operating frequency is the bias circuit requirements. Designing an on-chip bias circuit for monolithic traveling-wave amplifiers with bandwidths over several octaves without degrading their flat gain performance represents a severe design problem.

Distributed transmission-line sections exhibit several res-

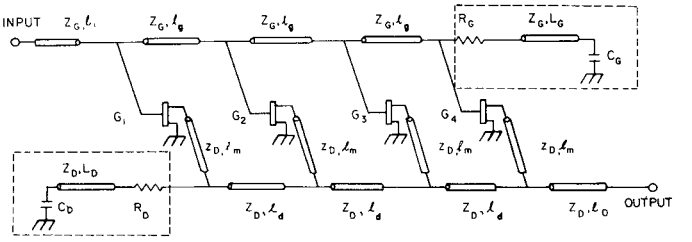


Fig. 1. Schematic representation of a four-stage FET traveling-wave preamplifier.

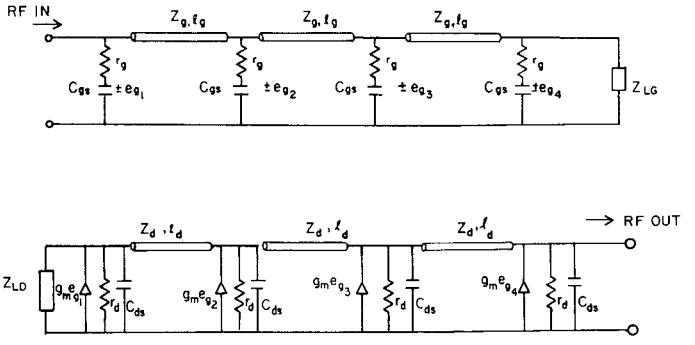


Fig. 2. Simplified equivalent circuit diagram of a GaAs FET traveling-wave preamplifier.

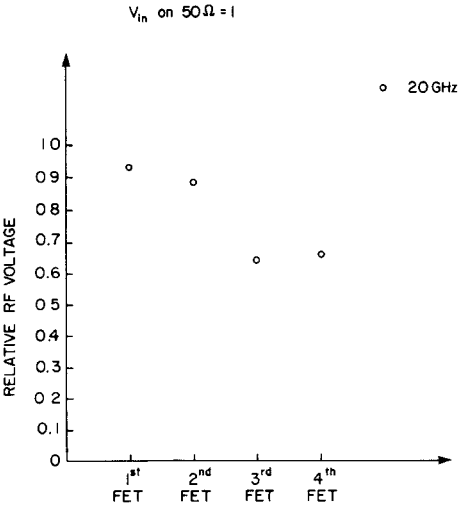


Fig. 3. Relative RF voltage distribution on the gate line at 20 GHz.

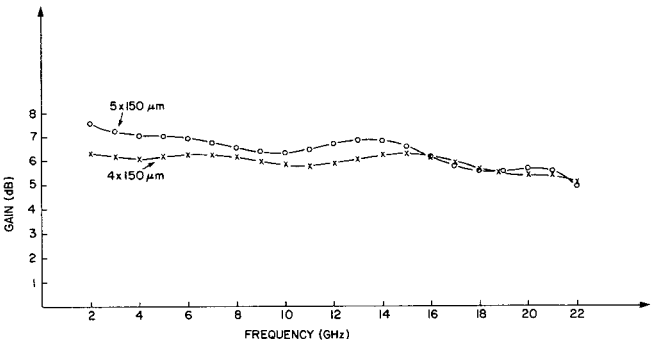
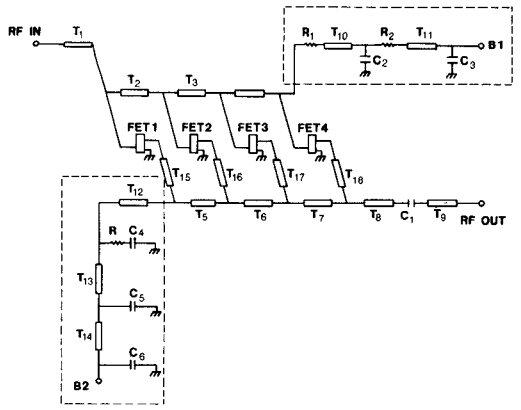


Fig. 4. Comparison of gain predictions for four-cell and five-cell designs.



DESCRIPTION OF CIRCUIT COMPONENTS

T_1, T_8, T_9	Input and output matching transmission-line sections
T_2, T_3, T_4	Gate-line transmission-line sections
T_5, T_6, T_7	Drain-line transmission-line sections
T_{10}, T_{11}	Transmission-line sections for gate-bias circuitry
T_{12}, T_{13}, T_{14}	Transmission-line sections for drain-bias circuitry
$T_{15}, T_{16}, T_{17}, T_{18}$	rf matching transmission-line sections
C_1	dc blocking capacitor
C_2, C_3	Gate-bias circuitry rf bypass capacitors
C_4, C_5, C_6	Drain-bias circuitry rf bypass capacitors
R_1, R_2	Gate-bias circuitry resistors
R_3	Drain-bias circuitry resistor
FET 1 to FET 4	150 μm gate periphery MESFETs
B1	Gate dc bias terminal
B2	Drain dc bias terminal

Components with a bar on top refer to the second stage

Fig. 5. Schematic circuit design for the single-stage small-signal amplifier, with gate and drain bias circuits included.

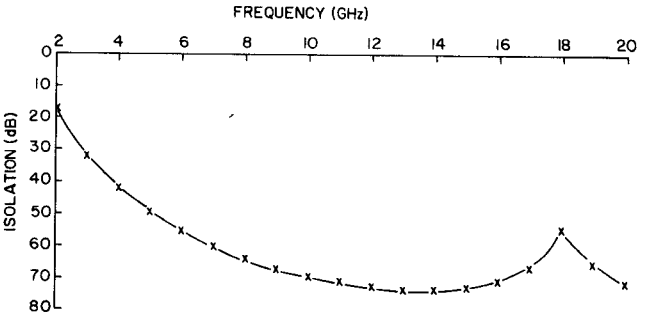


Fig. 6. Isolation performance of the drain bias circuit.

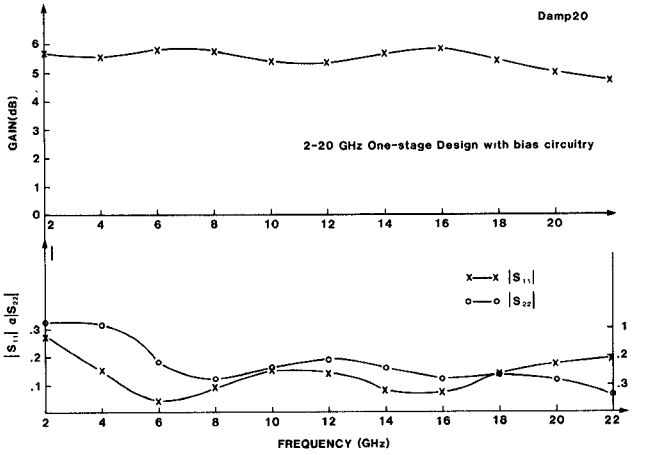


Fig. 7. Predicted performance of the single-stage 2–20-GHz amplifier.

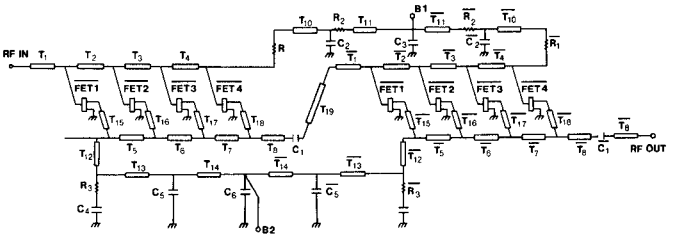


Fig. 8. Schematic circuit design for the two-stage small-signal amplifier. Description of the circuit components is identical to Fig. 5.

onances or impedance variations as frequency of operation is varied so that, for example, what may be a short transmission-line section at 2 GHz can become over a wavelength long at 20 GHz.

We have addressed this problem in our 2–20-GHz amplifier development work. The basic circuit diagram for an amplifier without the bias circuitry appears in Fig. 1. Both the gate and drain lines need to be terminated by complex impedances, as shown inside the dashed-line rectangles. In our approach, the complex terminating impedances are replaced by the circuits shown inside the dashed-line rectangles in Fig. 5. These circuits perform the following three functions.

1) They present the correct complex impedances to the gate and drain lines, respectively.

2) They isolate the dc-bias ports *B*1 and *B*2 from RF signals. It is most difficult to achieve isolation at the low end of the frequency band because of the limited value of inductances and capacitances one can realize monolithically. To illustrate this point, the isolation performance of the drain bias circuit is plotted in Fig. 6. Although isolation decreases steadily toward 2 GHz, we were able to obtain a minimum of 17-dB isolation and still limit the largest capacitor value to 10 pF.

3) These circuits allow the dc currents to pass without power dissipation. This requirement is not necessary for the gate bias circuit, and therefore series resistances are allowed there. These resistances stabilize the circuit at very low frequencies and inhibit any tendency toward bias circuit oscillation.

Fig. 7 shows the predicted performance of the single-stage amplifier, including the effect of bias circuitry. The gain is 5.5 ± 0.5 dB, and both the input and output return loss are better than 10 dB across the full frequency band.

The basic single-stage design is used as the building block for the two-stage design, as shown in Fig. 8. Because each section is well matched for the 50-Ω system, a complicated interstage matching circuitry is not required. Gate and drain bias circuits of each stage are connected to the same dc gate and drain bias ports, respectively. In this connection, capacitances C_3 and C_5 are shared between the two circuits. The sum of all the capacitors in the circuit is less than 56 pF for the two-stage. The dc blocking capacitors are included in series with the drain output RF line to allow direct cascading of individual chips. The dc blocking capacitors have 2-pF values, and the maximum value of any capacitor used in the circuit is 10 pF.

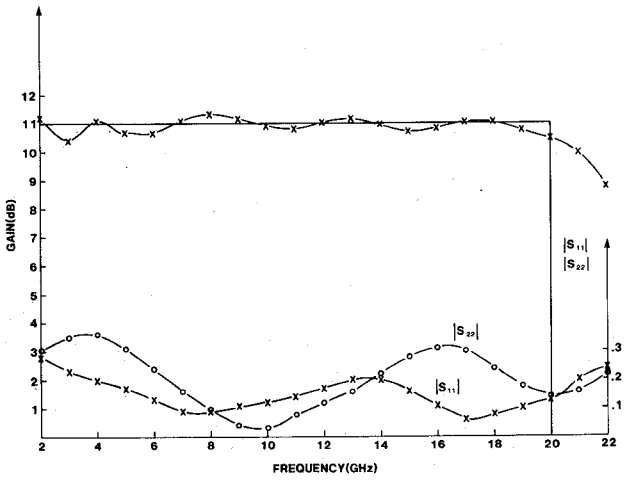


Fig. 9. Calculated performance of the two-stage 2–20-GHz amplifier.

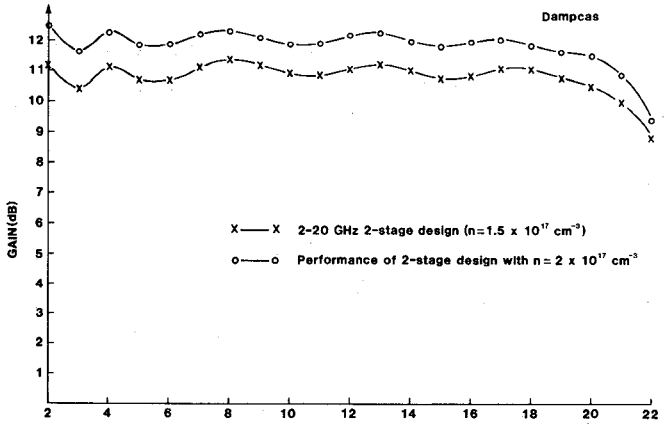


Fig. 10. Comparison of different doping levels for the predicted two-stage amplifier design.

The calculated performance of the two-stage amplifier is shown in Fig. 9. The gain is 11 ± 0.5 dB, and the input and output return loss is around 10 dB across the full band.

With an 11-dB gain per two-stage amplifier, the minimum of 34-dB isolation that is expected through the common bias circuitry is quite satisfactory. The performance of the amplifier has been checked with the full circuitry shown in Fig. 9 for any sign of feedback effects in and outside the design band.

We have also examined the effect of channel doping on the amplifier performance, the original circuit optimization employed on an FET model with 1.5×10^{17} cm^{-3} doping level. If the FET equivalent circuit is scaled to 2×10^{17} cm^{-3} and inserted in the design without other circuit changes, no degradation in performance is observed. Only the gain increases, about 1 dB, representing the increased g_m. The insensitivity of the design–to–channel doping is a good indication of the stability of the circuit. Fig. 10 compares the performances of two different doping levels.

III. Circuit Description and Experimental Results

The single-stage circuit is realized on a 2.2×2.7 mm (86×106 mil) chip (Fig. 11). There are four FET cells, each with two 75-μm width gate fingers, for a total gate periphery of 600 μm.

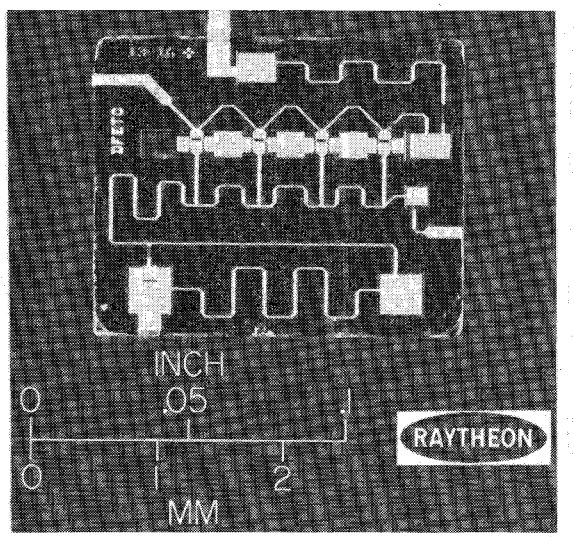


Fig. 11. Single-stage, 2–20-GHz amplifier chip.

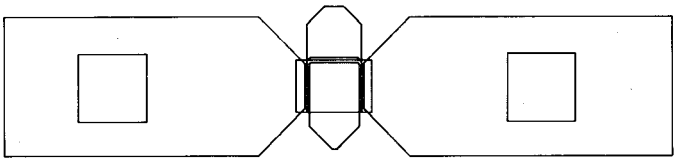


Fig. 12. Layout for the 2–20-GHz amplifier 2×75-μm discrete FET.

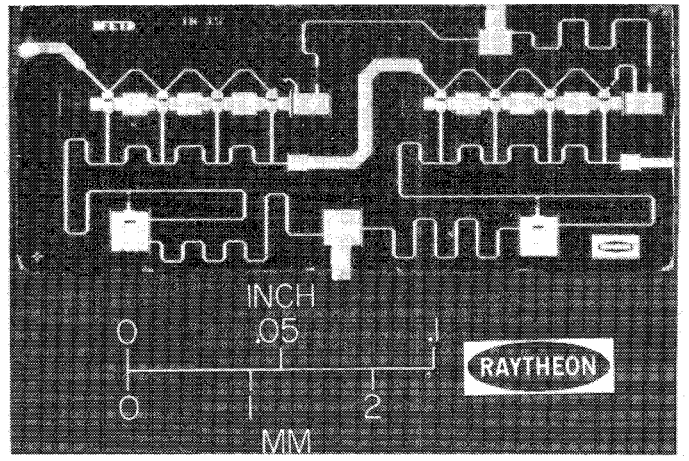


Fig. 13. Two-stage preamplifier chip.

The discrete FET layout is shown in more detail in Fig. 12; note that gate and drain pads are made large enough to allow automatic dc probing. In these devices, the gate length varied between 0.8 and 0.9 μm. The circuits are fabricated using our standard MMIC technology, which has been described in detail previously [6]. All capacitors are thin-film Si_3N_4 and the resistors are thin-film titanium.

The circuit shown schematically in Fig. 8 is realized on a single 2.2×5.5 mm (80×216 mil) chip (Fig. 13). Total gate periphery is just double that of the single-stage amplifier.

The measured performance of the single-stage amplifier is presented in Fig. 14. Gain is 6 ± 1.5 dB in the 2–22-GHz frequency range.

We have found the measured gain flatness to be typically in the ± 1-dB range over the 2–20-GHz frequency range.

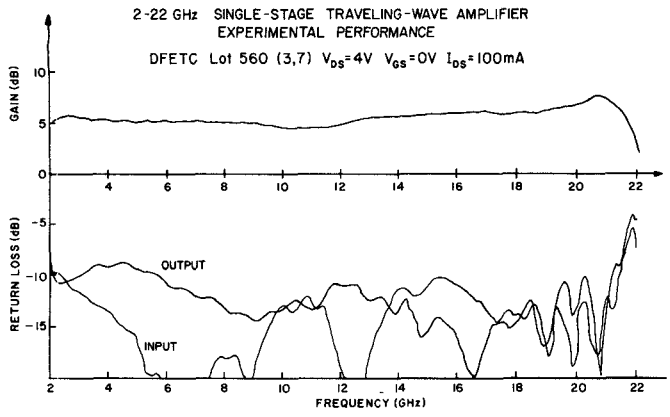


Fig. 14. Experimental performance of the 2–22-GHz single-stage traveling-wave amplifier.

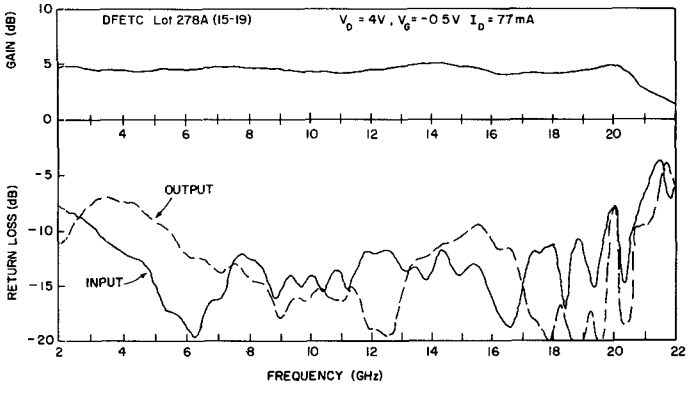


Fig. 15. Performance of the 2–20-GHz single-stage amplifier with best measured gain ripple performance. Gain ripple is ±0.5 dB in the 2–20.6-GHz band.

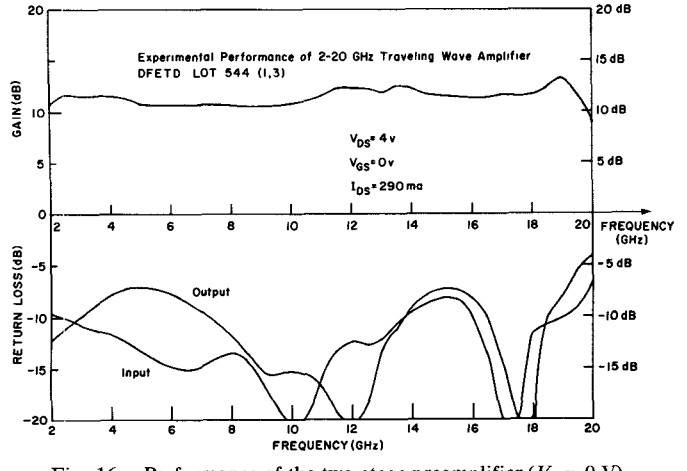


Fig. 16. Performance of the two-stage preamplifier (V_G = 0 V).

Gain flatness is ±0.5 dB on our computer simulations. The best performance in terms of gain flatness measured so far is ±0.5 dB between 2 and 20.6 GHz, as shown in Fig. 15. Input and output return losses are generally 10 dB or better across the band. On some chips, however, we have measured return losses as low as 7 dB at certain frequencies.

The measured performance of the two-stage amplifier with V_G = 0 V (Fig. 16) shows gains in the 11–13-dB range. Isolation of the input from the output is better than −50 dB at the low end, and better than −30 dB at the high end

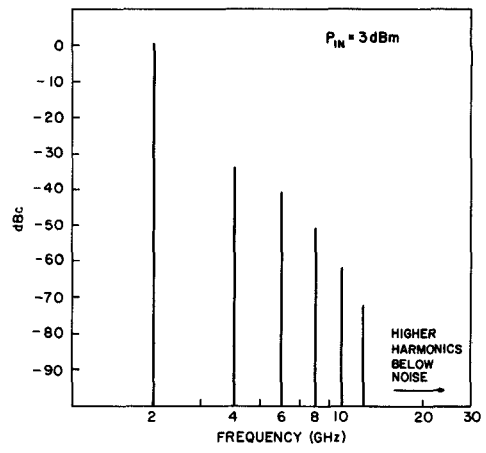


Fig. 17. Harmonics of 2-GHz input signal (P_{in} = 3 dBm).

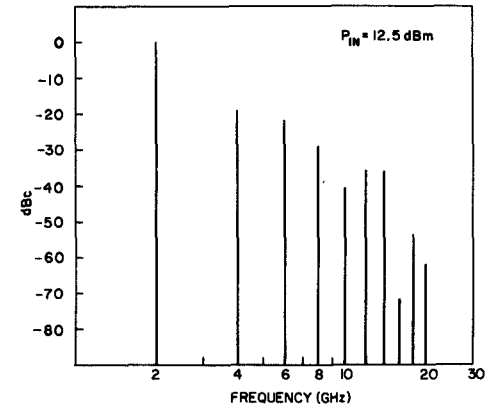


Fig. 18. Harmonics of 2-GHz input signal at 3.5-dB gain compression (P_{in} = 12.5 dB).

of the frequency band. Fig. 16 also shows input and output return loss. Output return loss seems higher than both the predicted value and the measured single-stage results.

Both the single-stage and two-stage designs include the full gate and drain bias circuitry plus the output dc blocking capacitors on the chip. Therefore, the flat gain responses we have measured have the additional significance that the bias circuitry is also functioning properly, without producing resonances or absorption of power across such an extremely wide band.

No data on third-order intermodulation products is available at present for 2–20-GHz amplifiers. However, harmonics of the input signal were recorded for the two-stage preamplifier. For a 2-GHz input signal, all harmonics up to the tenth are in the passband of the amplifier. Fig. 17 shows these higher harmonics for a 2-GHz input signal below the gain compression of the amplifier (P_{in} = 3 dBm), and Fig. 18 shows the same at more than 3-dB gain compression (P_{in} = 12.5 dBm). Even at high gain compression levels, the second harmonic component is 19-dB below the carrier, representing excellent linearity.

We have also measured the noise performance of the amplifier. Fig. 19 shows the noise performance of the single-stage amplifier. The noise figure is 7±1 dB across the full 2–18-GHz frequency band at maximum gain condition. This noise figure includes the input dc block and jig losses.

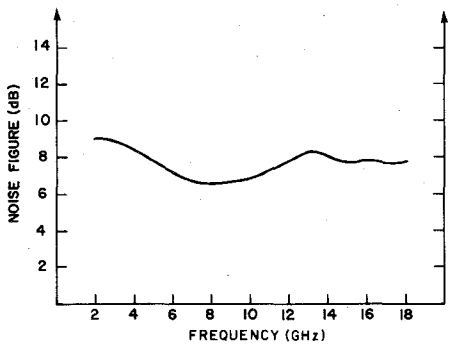


Fig. 19. Single-stage 5-dB gain preamplifier noise performance ($V_G = 0$ V).

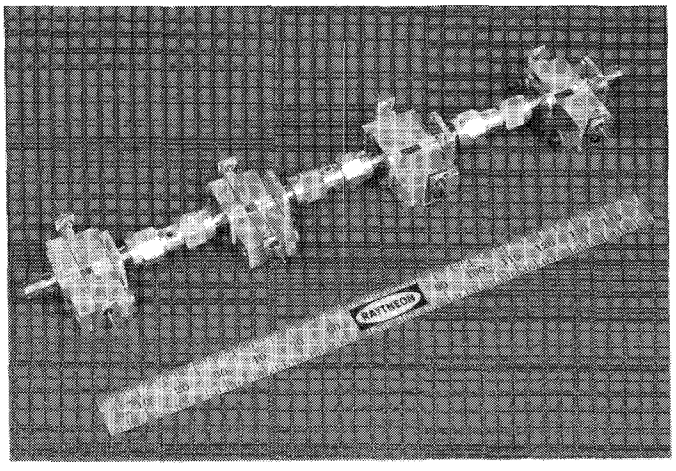


Fig. 20. Cascaded 2–20-GHz amplifier which achieved 30-dB gain.

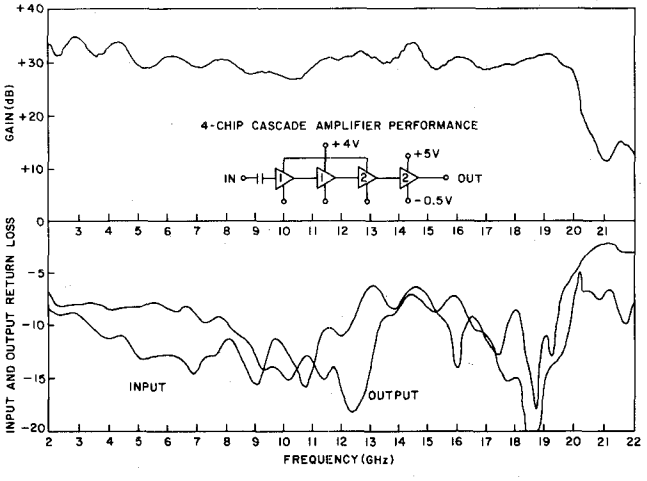


Fig. 21. Cascaded amplifier performance.

To demonstrate that traveling-wave amplifiers can be cascaded and that 30-dB gains in the 2–20-GHz band are feasible, we have cascaded six preamplifier stages. We are pleased to report that we have achieved gains around 30 dB across the full 2–20-GHz frequency band. The cascaded amplifier chain (Fig. 20) consists of two single-stage and two two-stage preamplifier chips, cascaded in separate jigs. The performance of the amplifier is shown in Fig. 21. Gain performance is around 30 dB with ±4-dB gain ripple. We believe that some of the gain ripple is contributed by the jigs and the transitions employed in cascading. Input and output return loss is better than −6 dB.

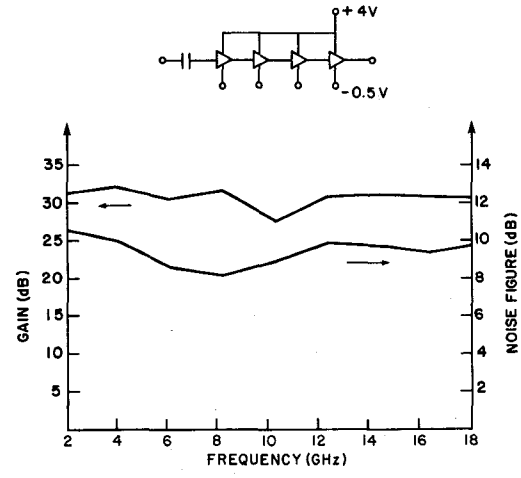


Fig. 22. Noise figure performance of the 30-dB cascaded amplifier. Jig and dc block losses are not taken out.

The noise performance of the amplifier is also measured. The data shown in Fig. 22 indicates a noise figure of 9±1 dB in the 2–18-GHz frequency band. This noise figure includes the input dc block and jig losses. The measurement was performed at maximum gain condition. We have not observed significant improvement in the noise figure by biasing the gates negatively.

IV. Conclusion

Extremely wideband traveling-wave amplification is shown to be possible with GaAs monolithic technology. Decade-band 2–20-GHz single- and two-stage GaAs traveling-wave amplifiers with 6- and 12-dB flat gains are realized in single-chip form with full on-chip dc biasing circuitry and dc blocking capacitors. The initial experimental results are in excellent agreement with the theoretical predictions.

By cascading these amplifiers, a 30-dB gain across the 2–20-GHz frequency band is achieved with a noise figure of 9±1 dB.

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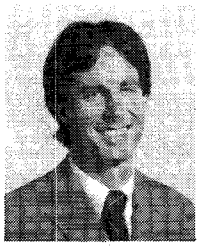

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